PY32F410 Datasheet

32-bit ARM® Cortex®-M4 Microcontroller

Puya Semiconductor (Shanghai) Co., Ltd.

Features

- Core
  - 32-bit ARM® Cortex® -M4 processor core supporting DSP instructions
  - Frequency up to 128 MHz
- Memories
  - 128 KB of dual bank Flash (Supports Read-While-Write)
  - 16 KB of SRAM
- Clock, reset and power management
  - 2.0 to 3.6 V
  - Power-on/power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - 4 to 32 MHz high-speed external crystal oscillator (HSE)
  - Embedded 8/16/24/48 MHz high-speed oscillator (HSI)
  - 32.768 kHz low-speed external crystal oscillator (LSE)
  - 40 kHz low-speed internal RC oscillator (LSI)
  - PLL supports CPU up to 128 MHz and PWM up to 144 MHz (f_{HCLK} = 72 MHz)
- Low-power mode
  - Sleep, Low-power run, Low-power sleep and Stop0/1/2 modes
  - Backup register (20 Bytes)
- 1 x 12 bit ADC
  - Up to 16 external input channels
  - Conversion range: 0 to V_{REF+}
  - Single-ended or differential input
  - Supports sampling time and resolution configuration
  - Supports single-shot, continuous, scan and discontinuous conversion modes
  - Temperature sensor
  - Voltage sensor
- 2 x analog comparators
- 2 x operational amplifiers (OPA2 can be used as a comparator)
- 8-channel DMA controller
  - Supported peripherals: Timer, ADC, UART, I^2C, I^2S and SPI
- Up to 60 I/Os:
  - All mappable on 16 external interrupt vectors
  - Some ports support 5 V-tolerant
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- Up to 17 timers
  - 1 x 16-bit advanced-control timers, having 4-channel PWM timers with dead-time generation and emergency stop
  - 1 x 32-bit, 5 x 16-bit general-purposed timers with up to 4 independent channels for input capture/output comparison, the general-purposed timers also support encoder interfaces using two inputs of quadrature decoders
  - 1 x 16-bit low power timer
  - 2 x 16-bit basic timers
  - 2 x watchdog timers (Independent and Window)
  - 1 x SysTick: 24-bit self-decrement counter
  - 4 x independent PWM modules each supporting 4-channel PWM output
  - Up to 36 timer and PWM independent channels
- RTC
- Up to 8 communication interfaces
  - 1 x LPUART, 1 x USART, 2 x UART interfaces
  - Up to 2 x I^2C interfaces
  - Up to 2 SPIs
- 96-bit unique ID (UID)
- Packages: LQFP64, LQFP48, QFN48 and QFN32

Content

1. Introduction

The PY32F410 devices are based on the high-performance Arm® Cortex®-M4 32-bit core. It is embedded with up to 128 KB Flash and 16 KB SRAM memory, up to 128 MHz and available in multiple package options. The PY32F410 integrates multi-channel I^2C, SPI, USART and other communication peripherals, one 12-bit ADC and 17 timers.

The PY32F410 microcontrollers operates across a temperature range of -40 to 105 °C and a standard voltage range of 2.0 to 3.6 V. The device provides Sleep, Low power run, Low power sleep and Stop low power operating modes, which can meet different low-power applications.

The PY32F410 series microcontrollers are suitable for various applications such as motor control, industrial applications, kitchen and bathroom appliances, and smart home systems.

Table 1-1 PY32F410 series product features and peripheral counts

Peripherals		PY32F410R1BT7	PY32F410C1BT7	PY32F410C2BU7	PY32F410K1BU7
Flash (KB)		128	128	128	128
SRAM (KB)		16	16	16	16
Timers	General-purpose	6			
	Advanced-control	1			
	SysTick	1			
	Basic	2			
	LPTIM	1			
	Watchdog	2			
	RTC	1			
	PWM	4			
Comm. interfaces	USART	1			
	UART	2			
	LPUART	1			
	I^2C	2			
	SPI (I^2S)	2 (2)			
DMA		8ch			
GPIO		60	44	45	31
ADC	Number	1	1	1	1
	Channels (external + internal)	16+5	10+5	16+5	10+5
Comparators		2			
Operational Amplifiers(1)		2	1	2	1
Max. CPU frequency		128 MHz (CPU)/144 MHz (PWM)			
Operating voltage		2.0 to 3.6 V			
Operating temperature		-40 to 105 °C			
Packages		LQFP64	LQFP48	QFN48	QFN32

1. When there are two operational amplifiers OPA1/OPA2, OPA2 can be used as a comparator.

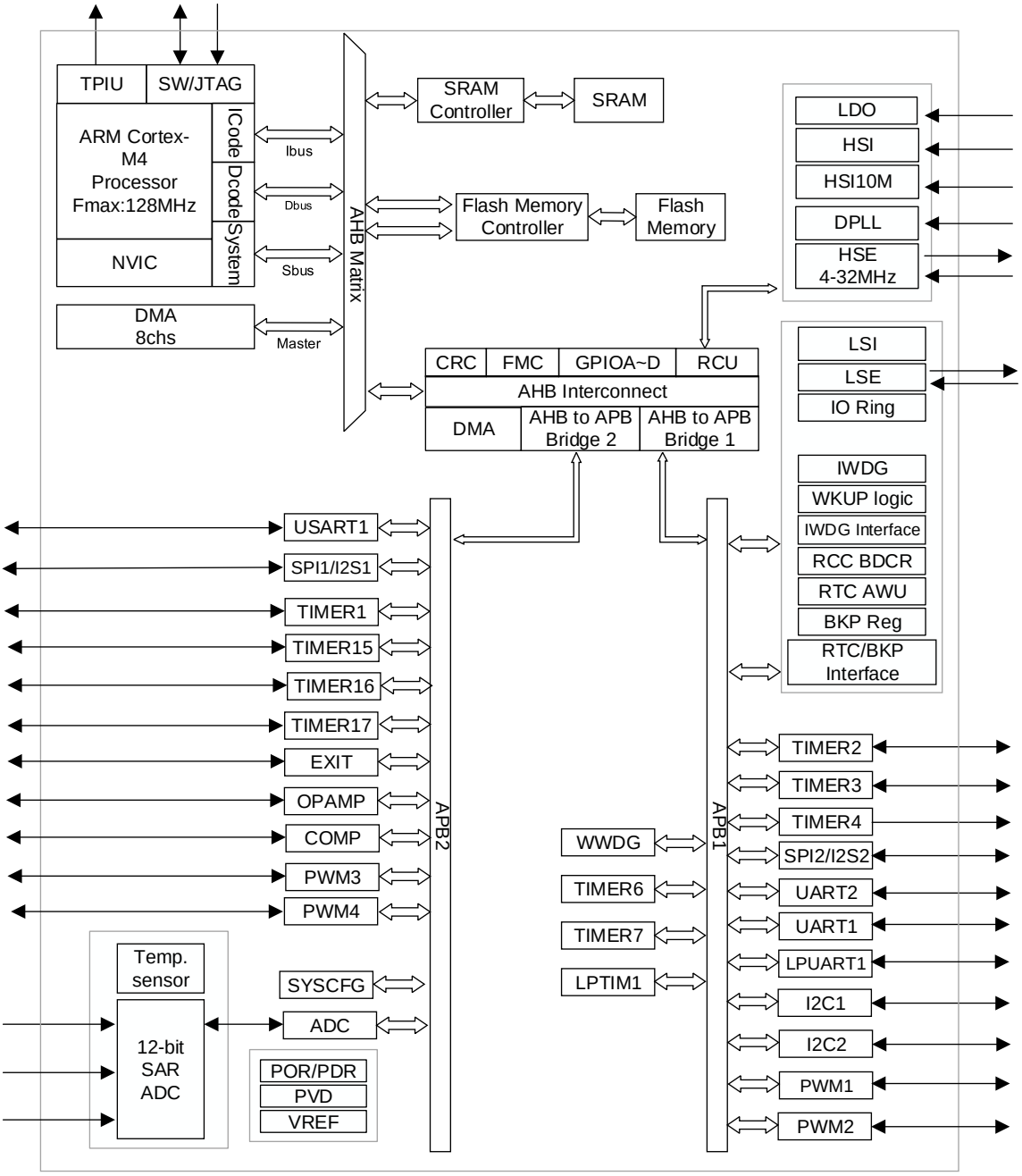


Figure 1-1 System block diagram

2. Functional overview

2.1. ARM ® Cortex ® M4 Processor

The Arm® Cortex®-M4 32-bit RISC processor with DSP instructions features an exceptional code-efficiency, delivering the expected high-performance from an Arm core in a memory size usually associated with 8-bit and 16-bit devices. The processor supports a set of DSP instructions, which allow efficient signal processing and complex algorithm execution. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. It is compatible with all Arm tools and software.

32-bit ARM ® Cortex® -M4 processor

- Supports 128 MHz operating frequency
- Single cycle multiplier and hardware divider
- Integrated DSP instructions
- Nested vectored interrupt controller (NVIC)
- 24-bit SysTick timer

The ARM ® Cortex®-M4 processor is based on the ARMv7-M architecture and supports Thumb and Thumb-2 instruction sets.

- The internal bus matrix connects the I-Code bus, D-Code bus, system bus, private peripheral bus (PPB), and debug access (AHB-AP).
- Nested vectored interrupt controller (NVIC)
- Flash patch and breakpoint (FPB)
- Data watchpoint and trace (DWT)
- Instrumentation trace macrocell (ITM)
- Serial wire JTAG debug port (SWJ-DP)
- Trace port interface unit (TPIU)
- Memory protection unit (MPU)

2.2. Memories

Embedded up to 16 KB SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The start address of the SRAM is 0x2000 0000.

The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data
- 5 KB of Information area:
  - Option bytes

- UID bytes
- OTP
- System memory

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) blocks external access.
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.

2.3. Boot modes

At startup, the BOOT0 and option bytes are used to select one of the three boot options in the following table :

Table 2-1 Boot configuration

Boot mode configuration					Mode
BOOT_Lock	nBOOT1 FLASH_OPTR2[8]	nBOOT0 FLASH_OPTR2[14]	BOOT0 Pin	nSWBOOT0 FLASH_OPTR2[13]	
1	X	X	X	X	Boot from Main flash
0	X	X	0	1	Boot from Main flash
0	X	1	X	0	Boot from Main flash
0	0	X	1	1	Boot from SRAM
0	0	0	X	0	Boot from SRAM
0	1	X	1	1	Boot from System flash
0	1	0	X	0	Boot from System flash

The Boot loader is located in the system memory and is used to reprogram the Flash memory by using USART or UART interface.

2.4. Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4G bytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and act. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed. The MPU is optional and can be bypassed for applications that do not need it.

2.5. Flash accelerator (ACC)

To release the processor full performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the flash memory.

Based on the CoreMark benchmark, the performance achieved thanks to the accelerator is equivalent to 0 wait state program execution from the flash memory at a CPU frequency up to 128 MHz.

- ICODE can prefetch instructions
- The instruction cache has 64 branches and the data bit width is 64 bits
- The data cache has 16 branches, and the data bit width is 64 bits

2.6. Backup Register (BKP)

Backup registers are 5 32-bit registers used to store 20 bytes of user application data. The module is in the backup domain and is supplied by the V_{CC}. It will be reset when the power reset (POR) or BDRST of the BDCR writes 1.

- Supports 20-byte data backup register
- Status/control register for managing anti-intrusion detection and having interrupt function
- A check register used to store the RTC check value.
- Output an RTC calibration clock, an RTC alarm pulse or a second pulse on the PC13 pin (when this pin is not used for intrusion detection)

2.7. Clock management

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- An 8/16/24/48 MHz internal high-precision configurable HSI clock
- A 40 kHz configurable internal LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock
- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, disable PLL and HSE, and the system clock is automatically switched to HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The AHB frequency is up to 128 MHz.

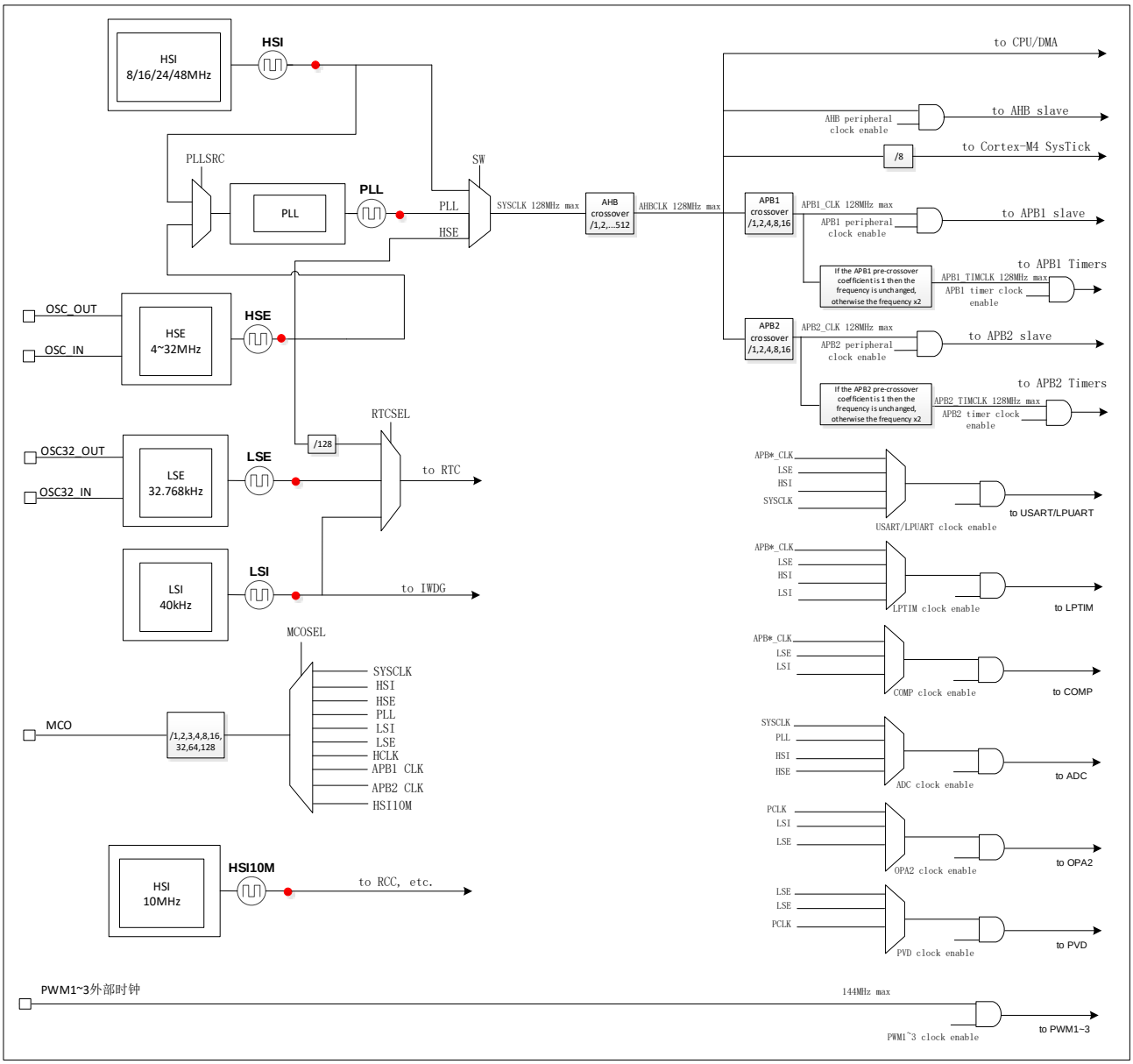


Figure 2-1 System clock structure diagram

2.8. Power management

2.8.1. Power block diagram

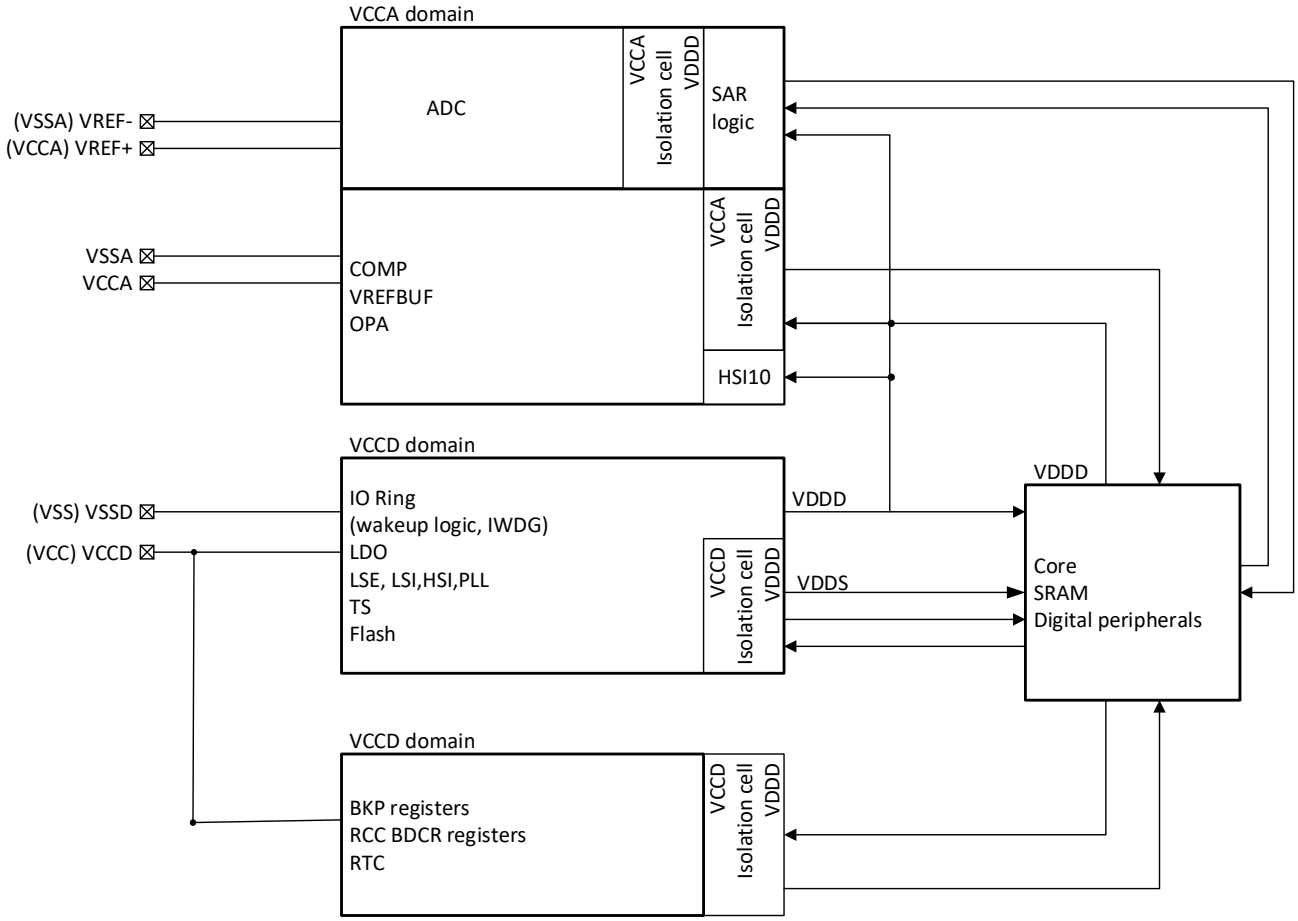


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	2.0 to 3.6 V	The power is supplied to the device through the power pins.
2	V_{CCA}	2.0 to 3.6 V	The power is supplied to the device through the power pins, with the power supply module comprising: Partial analog circuits
3	V_{DDD}	1.2 V (Default)	VR supplies power to the main logic circuits and SRAM inside the chip. Three modes: MR, LPR, and DLPR can be selected.

2.8.2. Power monitoring

2.8.2.1. Power-on/power-down reset (POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed to provide power-on and power-down reset for the device. The module keeps working in all modes.

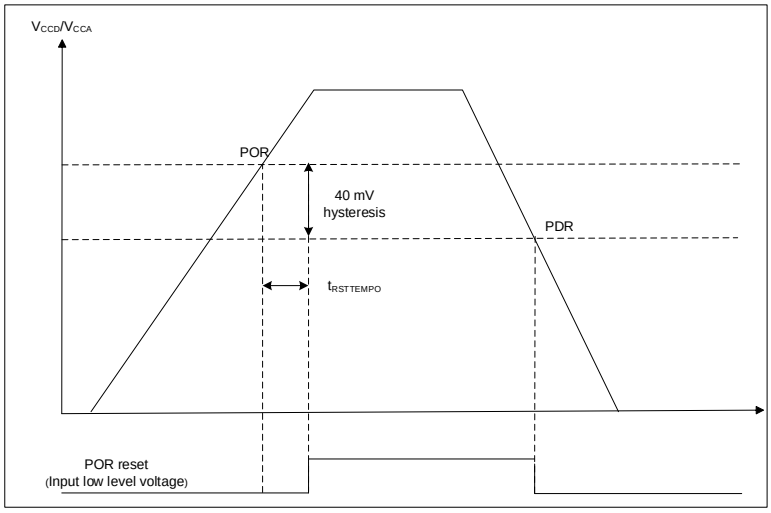


Figure 2-3 POR/PDR thresholds

2.8.2.2. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply and the detection point is configured through the register. When V_{CC} is higher or lower than the detection point of PVD, the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

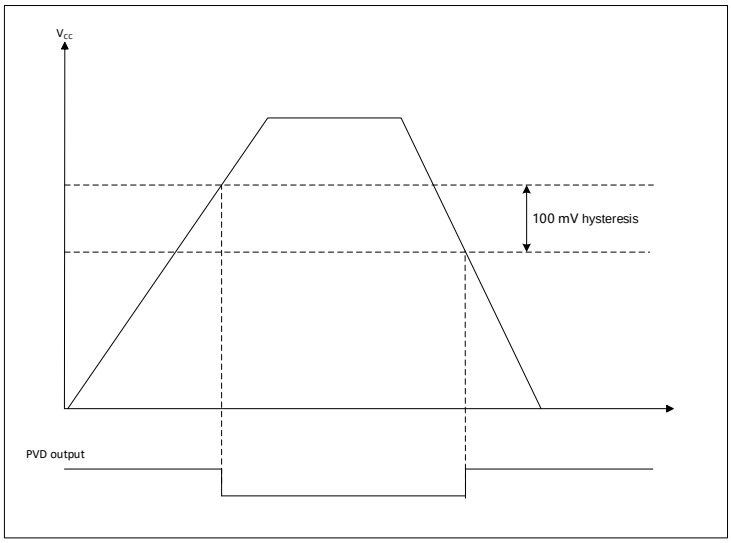


Figure 2-4 PVD threshold

2.8.3. Voltage regulator

The regulator has three operating modes:

- Main regulator (MR) is used in Run mode.
- Low power regulator (LPR) provides an option for even lower power consumption.
- Deep low power regulator (DLPR) ensures the lowest power consumption in low power mode.

2.8.4. Dynamic voltage scaling management

The device incorporates an embedded linear regulator, that is the main regulator (MR), which powers most digital circuits. The main regulator operates in both Run mode and Sleep mode.

The device supports dynamic voltage scaling functionality to optimize power consumption during Run mode. The output voltage of the main regulator supplying the logic circuits can be dynamically adjusted according to the system's maximum operating frequency.

The main regulator (MR) operates within the following ranges:

- **High-voltage (Range 1) mode**: Supports maximum CPU frequencies up to 128 MHz
- **Medium-voltage (Range 2) mode**: Supports maximum CPU frequencies up to 96 MHz
- **Low-voltage (Range 3) mode**: Supports maximum CPU frequencies up to 64 MHz

2.8.5. Low-power mode

In addition to the Run mode, the device has four low-power modes:

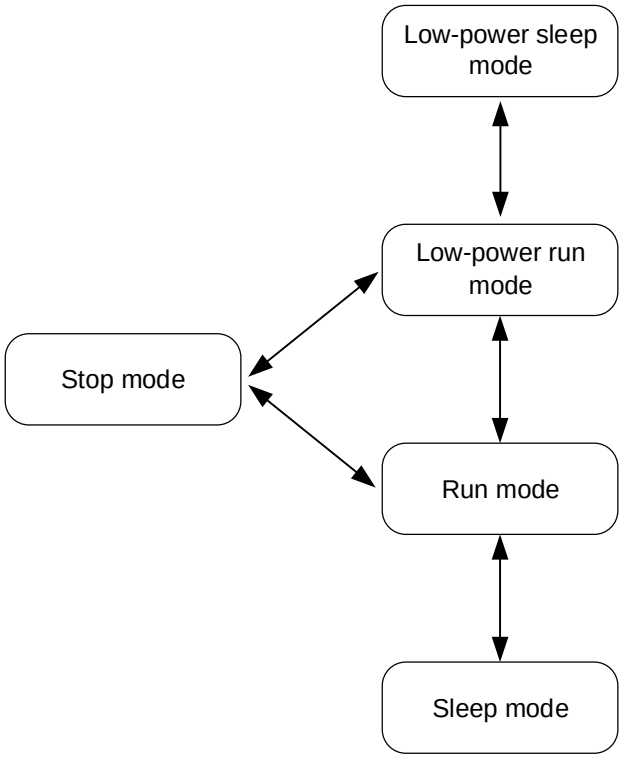


Figure 2-5 Low-power mode

- **Sleep mode:** Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- **Low-power run:** In this mode, the CPU operating frequency is limited to 2 MHz, and peripheral modules with independent clocks can operate at HSI frequencies.
- **Low-power sleep mode**: entered only from Low-power run mode and CPU core clock is turned off. The system returns to Low-power run mode when awakened by an event or interrupt.

- **Stop0/Stop1/Stop2 mode**: In this mode, SRAM and register contents are retained. PLL, HSI and HSE are turned off and most module clocks in the V_{DDD} domain are disabled. GPIO, PVD, I^2C, LPUART1, IWDG, Low-power timer, COMP and RTC can wake up the Stop mode.

2.8.6. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)

2.8.7. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Window watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.8.8. Backup domain reset

A backup domain reset will reset all backup domain registers, including RCC_BDCR, backup registers, and RTC partial registers.

A backup domain reset is generated when one of the following events occurs:

- Software reset, triggered by setting the BDRST bit in the RTC domain control register (RCC_BDCR).
- After the power supply V_{CC} has been powered down, it is powered on again.

2.9. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating，pull-up/down，analog) or as peripheral alternate function.The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers. OPA features are summarized as follows:

- Support read/write operations via IO Port or AHB bus
- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers (Max. 16 alternate functions for each IO)

- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions

2.10. DMA

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations. The device has two general-purpose dual-port DMAs with 8 channels. Each channel is dedicated to managing requests for memory access from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- Single AHB Master
- 8 configurable channels
- Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
- Priority between multiple requests on the same DMA module is software-programmable. For equal priorities, hardware resolves conflicts (lower channel number = higher priority).
- The transfer sizes of the source and destination are independent (byte, half word and word), simulating packing and unpacking. Source and destination addresses must be aligned to the transfer width.
- Programmable address modes: Increment, decrement, or fixed.
- Each channel has 4 event flags: transfer complete (circular mode), block transfer, half-block transfer and transfer error. They are logically ORed to generate a single interrupt request.
- Support transfers between memory to memory, peripheral to memory, memory to peripheral and peripheral to peripheral.
- SRAM, APB and AHB peripherals can act as source or destination. FLASH can only act as a source.
- Support single-trigger mode and four circular modes:
  - Peripheral address retained, memory address retained
  - Peripheral address reloaded, memory address retained
  - Peripheral address retained, memory address reloaded
  - Both addresses reloaded
- Single-trigger mode: Programmable transfer count (0 to 65,535)
- Circular mode: Infinite looping or finite looping (1 to 255 cycles)
- Support single transfer and bulk transfer
- Single transfer: Generates 1 ACK per data transfer.

- Bulk transfer: Generates 1 ACK after all configured data is transferred (bus released post-completion).
- Two transfer modes
- Fast mode: Holds the bus until all data is transferred.
- Round-robin mode: Releases the bus after each transfer for re-arbitration.
- Support pausing transfers upon entering the block transfer Complete interrupt in circular mode.

2.11. Interrupts and events

The PY32F410 handles exceptions through the Cortex-M4 processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.11.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M4 processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M4 internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table , stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 8 interrupt priority
- Support 1 NMI
- Support 53 maskable external interrupts
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.11.2. Extended interrupt/event controller (EXTI)

- EXTI adds flexibility to handle physical wire events and generates wake-up events from GPIO and dedicated modules (PVD/RTC/COMP1/COMP2).
- The EXTI controller supports multiple channels with 20 configurable lines, including up to 60 GPIOs sharing 16 EXTI lines through multiplexing, along with a PVD output, RTC wake-up signals, and COMP1/COMP2 outputs. GPIO, PVD, RTC, COMP1 and COMP2 can be configured

to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channels through signal selection, with four direct input lines including I2C1, I2C2, LPTIM, and LPUART wake-up signals.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.12. Comparators (COMP)

The chip integrates two general-purpose comparators (COMP), namely COMP1 and COMP2. The COMP1/2 module can be used as a separate module or in combination with timer. The comparator can be triggered by analog signals to generate low-power mode wake-up functionality, supports analog signal conditioning, and when connected to PWM outputs from timers, enables cycle-by-cycle current control loops. The main features are as follows:

- Voltage comparison function is supported. Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - 256 steps voltage of V_{CCA}/V_{REFBUF} (i.e. V_{REFCMP})
  - Temperature sensor output
- Programmable speed and power consumption
- Rail to Rail
- Programmable hysteresis function
- Write protection for configuration registers (LOCK function)
- The output can be triggered by a connection to the I/O or timer input
- Each COMP has interrupt generation capability and is used to wake up the chip from low power mode (Sleep/Stop) (via EXTI)
- Provides software to configure the digital filtering time to enhance the anti-interference capability of the chip
- It supports output blanking to reduce switching noise.
- Support the Window Comp function

2.13. Operational amplifier (OPA)

Two operational amplifiers are embedded, each has two inputs and one output. Three I/Os can be connected to external pins, enabling any type of external interconnection.

The output is connected to the internal ADC. The main features are as follows:

- Rail-to-rail input and output voltage ranges
- Low input bias current

- Low input offset voltage
- High frequency gain bandwidth
- Comparator mode

2.14. Timer (TIMx)

Table 2-3 Timer characteristics

Timer type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
Advanced-control timer	TIM1	16-bit	up, down up/down	1 to 65536	Yes	4	3
General-purpose timers	TIM2	32-bit	up, down up/down	1 to 65536	Yes	4	-
	TIM3	16-bit	up, down up/down	1 to 65536	Yes	4	-
	TIM4	16-bit	up, down up/down	1 to 65536	Yes	4	-
General-purpose timers	TIM15	16-bit	up	1 to 65536	Yes	2	1
General-purpose timers	TIM16/TIM17	16-bit	up	1 to 65536	Yes	1	1
Basic	TIM6/TIM7	16-bit	up	1 to 65536	Yes	-	-
Dedicated PWM	PWM	16-bit	up, down	1 to 65536	Yes	4	-

2.14.1. Advanced timer (TIM1)

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The six independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

The two independent channels can be used for:

- Output compare
- PWM generation (internal channel, for triggering of ADC)
- Single pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, TIM1/TIM8 have full modulation capability (0 to 100%).

One brake input places the output signal of the timer in a safe state.

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

2.14.2. General-purpose timers

2.14.2.1. TIM2/TIM3/TIM4

The general-purpose timers TIM2/TIM3/TIM4 are consist of 16-bit (TIM2 is 32-bit) auto-reload counters and a 16-bit prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.

- They can work with the TIM1 by the Timer Link.
- Support DMA function
- Ability to process quadrature (incremental) encoder signals
- The counter can be frozen in debug mode.

2.14.2.2. TIM15/TIM16/TIM17

- The general-purpose timer (TIM15, TIM16 and TIM17) is consist of a 16-bit auto-reload upcounter driven by a programmable prescaler.
- TIM15 features 2 (TIM16/TIM17 having one) channels for input capture/output compare, PWM or one-pulse mode output.
- TIM15/TIM16/TIM17 have complementary outputs with dead time.
- Interconnection between timer and timer is controlled by external signal (only supported by TIM15)
- Support DMA function

2.14.3. Basic timers (TIM6/TIM7)

- The basic timer TIM6/TIM7 is consist of a 16-bit auto-reload upcounter driven by their programmable prescaler respectively.
- 16-bit auto-reload counter
- Generate interrupt/DMA request on update event (counter overflow).

2.14.4. Dedicated PWM (PWM1/PWM2/PWM3/PWM4)

- The PWM timer is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- 4 independent channels for output comparison, PWM output.
- Support DMA function
- The module supports external triggering, complementary output, dead-time control, and brake functions (PWM1/PWM2/PWM3).
- PWM1/PWM2/PWM3 support 144MHz

2.14.5. IWDG

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion

due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by independent RC oscillator and can work in Stop mode.
- The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.
- The IWDG hardware mode can be enabled by option byte.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.14.6. WWDG

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.14.7. LPTIM

LPTIM is a 16-bit timer. The ability of LPTIM to wake the system from low-power modes makes it suitable for practical low-power applications. LPTIM introduces a flexible clock scheme that can provide the required functionality and performance while minimizing power consumption.

- 16-bit up counter
- It has a 3-bit prescaler with 8 possible division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Optional clocks include LSE, LSI and APB clock
- Support single-shot and continuous modes

2.15. Analog-to-digital converter (ADC)

The device has a 12-bit SARADC. The module supports up to 21 measurement channels, including 16 external channels and 5 internal channels (Vsense, V_{CC}/3, V_{REFINT}, OPA1, and OPA2), with conversion capabilities in one-shot, scan, discontinuous, or continuous modes.

- A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- An efficient low-power mode is implemented to allow very low consumption at low frequency.
- Interrupt requests are triggered by the following events: end of conversion, continuous conversion and analog watchdog threshold violation (converted voltage exceeds preset limits)
- ADC can be configured with 12-bit, 10-bit, 8-bit and 6-bit resolutions
- Maximum ADC sampling rate: 3 MSPS
- Supports self-calibration
- Support programmable sampling time

- The data register allows configurable data alignment
- Support DMA requests for regular channel data conversion
- Channels 0 to 5 can be configured as differential inputs, others are fixed as single ended
- The oversampler is equipped with a 16 - bit data register. The oversampling rate can be adjusted from 2 to 256, and the programmable data shift can reach up to 8 bits
- Data processing supports gain compensation and offset compensation.

2.16. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.17. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- The RTC counter clock source may be a LSE, LSI and HSE/128.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.18. Cyclic redundancy check calculation unit (CRC)

CRC computing unit is based on a fixed generation polynomial to obtain 32-bit CRC computing results. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. The CRC calculation unit contains a 32-bit data register:

- When writing to this register, it serves as an input register, allowing you to input new data for CRC calculation.
- When reading from this register, it returns the result of the previous CRC calculation.
- Each time data is written to the register, the calculation result is a combination of the previous CRC calculation result and the new one (CRC calculation is performed on the entire 32-bit word rather than byte by byte).
- You can reset the register CRC_DR to 0xFFFFFFFF by setting the RESET bit in the register CRC_CR. This operation does not affect the data in the register CRC_IDR

2.19. System configuration controller (SYSCFG)

The SYSCFG module provides the following functions:

- Enable and disable I²C Fm+ mode
- Mapping the initial program area according to different boot modes
- DMA peripheral channel selection control
- Analog input channel enable
- Enable and disable Noise filter for all GPIOs
- Enable/disable EXTI (External Interrupt) for all GPIOs
- Dual bank internal Flash Address mapping configuration
- Enable and disable PVD Lock
- Enable and disable Cortex-M4 LOCKUP

2.20. Debug support (DBG)

The MCU DBG module assists the debugger with the following functions:

- Support Sleep and Stop mode
- When the CPU enters the HALT mode, the control timer, watchdog and PWM stops counting or continues counting
- Block I2C1 and I2C2 SMBUS timeouts when the CPU is in HALT mode

The DBG register also provides chip ID encoding. This ID encoding can be accessed by a JTAG or SW debug interface, or by a user program.

2.21. Inter-integrated circuit interface (I²C)

The I²C (Inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I²C bus. It controls all I²C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode plus (Fm+).

I²C features:

- 2 x I²C interfaces, supporting Slave and Master modes
- Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
  - Fast Mode Plus (Fm+): up to 1 MHz
- As master
  - Generate clock
  - Generation of start and stop
- As Slave
  - Programmable I²C address detection
  - Dual-address capability that responds to two secondary addresses

  - Discovery of the stop bit
- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function
- Support SMBus
- Support low-power modes, wakes up from Stop mode

2.22. Universal synchronous/asynchronous receiver transmitter (USART)

The PY32F410 contains 1 universal synchronous/asynchronous receiver transmitter (USART) and supports ISO7816, LIN and IrDA.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate for shared transmit/receive
- Automatic baud rate detection
- Two internal FIFOs for transmitting and receiving data

- Each FIFO can be enabled/disabled by software and has a status flag
- Dual clock domain with PCLK-independent peripheral-specific core clock
- Programmable data sequence, shifting MSB or LSB first
- Programmable data length of 7, 8 or 9 bits
- Configurable stop bits (0.5,1,1.5 or 2 bits)
- The transmitter provides a clock for synchronous transmission
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control: RS232, RS485
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance

2.23. Universal asynchronous receivers/transmitter (UART)

The PY32F410 features two universal asynchronous receivers/transmitters (UARTs):

- Support 5/6/7/8/9-bit serial data
- Support 1/2 STOP bits (1/1.5 STOP bits for 5-bit data)
- Support sending address/data
- Support fixed parity check
- Support break frames
- Detect start bit errors
- Support programmable fractional baud rates
- Support SWAP function
- Support MSB FIRST endianness switching
- Full-duplex asynchronous communication
- NRZ standard format

2.24. Low-power universal asynchronous receivers/transmitters (LPUART)

The PY32F410 features a low power universal asynchronous receivers/transmitters (LPUART):

- Full - duplex asynchronous communication
- NRZ standard mode
- Programmable baud rate
- 32.768 kHz clock, baud rate range 300 to 9600. Higher baud rates require higher clock frequency support
- Supports transmit and receive FIFO, software can be enabled separately,
- Dual clock domains: PCLK and dedicated kernel clock
- Configurable word length (7/8/9 bits)
- Configurable MSB or LSB first shifting
- Configurable stop bits (1/2 bit)
- Single-wire half-duplex communication
- Support continuous DMA transfer
- Centralized DMA buffering in SRAM for byte reception/transmission
- Independent enable for transmission and reception
- Independent polarity control for Tx/Rx signals
- Interchangeable Tx/Rx pins
- Support hardware RS - 485/modem flow control
- Parity control: generates parity bit on transmission, checks on reception
- Four error detection flags:
- Interrupt sourcrs with flags:
- Support 5/6/7/8/9-bit serial data

2.25. Serial peripheral interface (SPI)

PY32F410 contains 2 SPIs. The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- Master mode frequency up to 64 MHz
- Slave mode frequency up to 36 MHz
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode

- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Support TI mode
- Interrupt-causing Master mode faults or overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability

I^2S features:

- 2 x I^2S bus interfaces with sampling rate 8 to 192 kHz
- Support master and slave mode, full duplex and simplex communications

The I^2S bus provides a standard communication interface for digital audio applications over a 3-wire serial line. Two I^2S bus interfaces operate at 16/32 bit resolution in master or slave mode, with pins multiplexed with SPI1 and SPI2. Support audio sampling frequencies of 8 to 192 kHz, and the accuracy error is less than 0.5%. A DMA controller is available for all I^2S interfaces.

2.26. Serial wire debug (SWD)

An ARM SWD interface allows serial debugging tools to be connected to the PY32F410.

3. Pinouts and pin descriptions

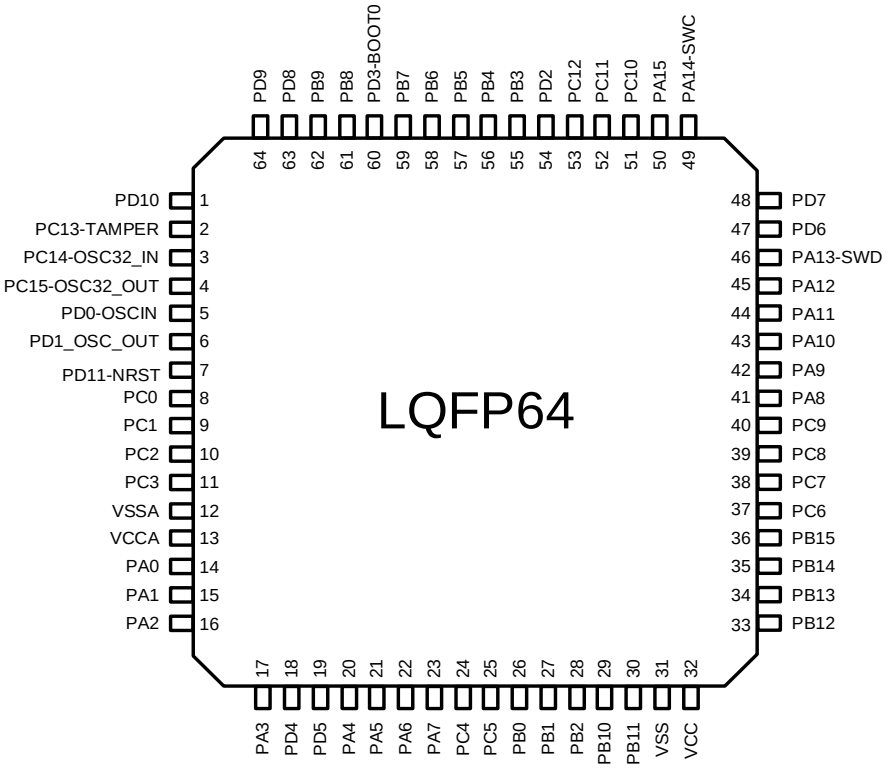


Figure 3-1 LQFP64 PY32F410R1xT7 Pinout1 (Top view)

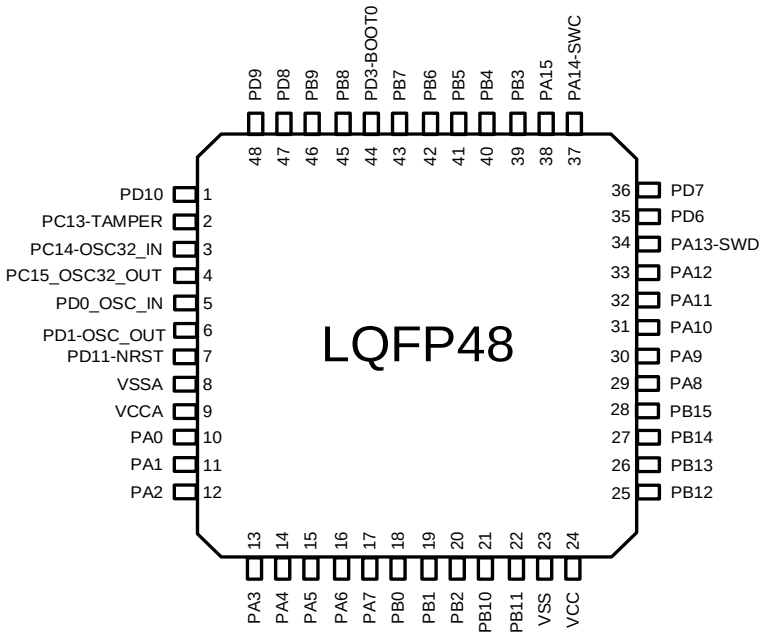


Figure 3-2 LQFP48 PY32F410C1xT7 Pinout1 (Top view)

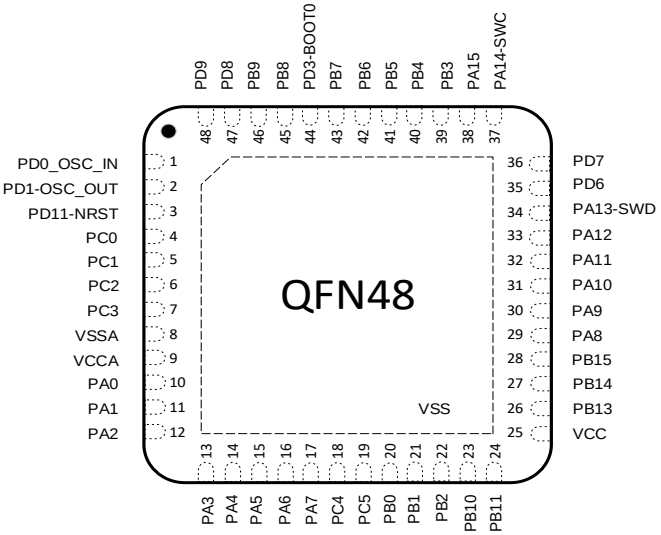


Figure 3-3 QFN48 PY32F410C2xU7 Pinout2 (Top view)

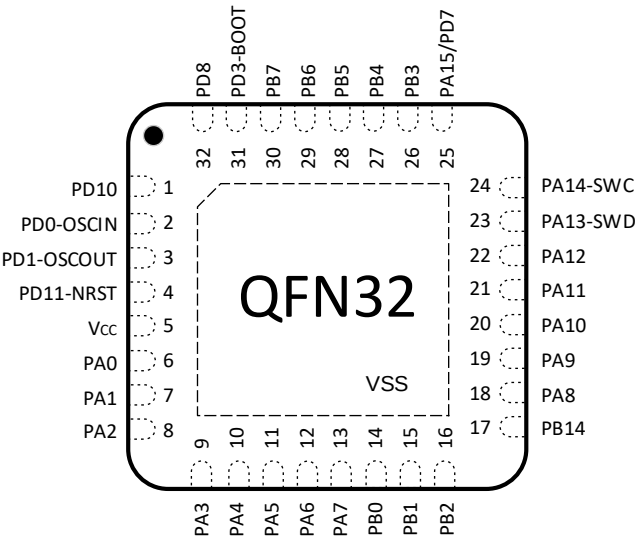


Figure 3-4 QFN32 (4 * 4) PY32F410K1xU7 Pinout1 (Top view)

Table 3-1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		NRST	Reset pin, low active
		I/O	Input/Output pins
		NC	No internal connection
I/O structure		FT	5 V tolerant I/O
		TT	3.3 V tolerant I/O
		TT_a	3.3 V tolerant with analog switch
		NRST	Reset port with internal weak pull-up resistor
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers or option bytes

Table 3-2 Pin definition[1][2]

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
1	1	-	1	PD10	I/O	FT	TIM4_CH4 PWM3_ETR_LS USART1_TX EVENTOUT	-
2	2	-	-	PC13-TAMPER	I/O	FT	PWM1_CH2 EVENTOUT	WKUP2 TAMP_RTC
3	3	-	-	PC14-OSC32_IN	I/O	TT	PWM1_CH3 EVENTOUT	OSC32_IN
4	4	-	-	PC15-OSC32_OUT	I/O	TT	PWM1_CH4 EVENTOUT	OSC32_OUT
5	5	1	2	PD0-OSC_IN	I/O	TT	TIM1_CH1 EVENTOUT	OSC_IN
6	6	2	3	PD1-OSC_OUT	I/O	TT	TIM1_CH2N SPI2_NSS/I2S2_WS EVENTOUT	OSC_OUT
7	7	3	4	PD11-NRST	NRST	NRST(FT)	MCO EVENTOUT	NRST
-	8	4	-	PC0	I/O	TT_a	I2C2_SCL I2C1_SCL PWM2_ETR_HS EVENTOUT	ADC_IN10
-	9	5	-	PC1	I/O	TT_a	I2C2_SDA SPI1_MOSI/I2S1_SD SPI2_MOSI/I2S2_SD I2C1_SDA PWM1_ETR_HS EVENTOUT	ADC_IN11
-	10	6	-	PC2	I/O	TT_a	SPI2_MISO I2S2_MCK PWM1_CH3 EVENTOUT	ADC_IN12

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
-	11	7	-	PC3	I/O	TT_a	SPI2_MOSI/I2S2_SD PWM1_CH3 EVENTOUT	ADC_IN13
8	12	8	-	V_{SSA}	G	-	-	-
9	13	9	-	V_{CCA}	S	-	-	-
10	14	10	6	PA0	I/O	TT_a	TIM2_ETR TIM2_CH1 COMP1_OUT TIM1_ETR TIM4_CH4 PWM1_ETR_LS UART1_RX LPUART1_TX EVENTOUT	ADC_IN0 COMP1_INM WKUP1
11	15	11	7	PA1	I/O	TT_a	TIM2_CH2 I2C2_SDA OPA2_COMP_OUT TIM15_CH1N I2C1_SMBA TIM4_ETR PWM1_BKIN PWM2_CH1 LPUART1_RX EVENTOUT	ADC_IN1 COMP1_INP OPA1_VINP
12	16	12	8	PA2	I/O	TT_a	TIM15_CH1 TIM2_CH3 COMP2_OUT PWM1_CH2 UART1_TX EVENTOUT	ADC_IN2 COMP2_INM OPA1_VOUT WKUP4
13	17	13	9	PA3	I/O	TT_a	TIM15_CH2 TIM2_CH4 I2C2_SCL I2S2_MCK PWM1_CH2N	ADC_IN3 COMP2_INP OPA1_VINM

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
							PWM2_BKIN UART1_RX EVENTOUT	
-	18	-	-	PD4	I/O	TT	I2C1_SDA TIM2_CH1 PWM2_CH3 EVENTOUT	-
-	19	-	-	PD5	I/O	TT	I2C1_SCL TIM2_CH2 PWM2_CH4 PWM3_CH1 EVENTOUT	-
14	20	14	10	PA4	I/O	TT_a	SPI1_NSS/I2S1_WS I2C1_SCL SPI2_NSS/I2S2_WS PWM1_CH1 EVENTOUT	ADC_IN4 COMP1_INM
15	21	15	11	PA5	I/O	TT_a	SPI1_SCK/I2S1_CK TIM2_ETR TIM2_CH1 OPA2_COMP_OUT LPTIM1_IN1 PWM1_CH1N UART2_RX USART1_CK EVENTOUT	ADC_IN5 COMP2_INM
16	22	16	12	PA6	I/O	TT_a	SPI1_MISO TIM3_CH1 TIM1_BKIN COMP1_OUT TIM16_CH1 I2S2_MCK TIM4_CH1 PWM1_ETR_HS PWM3_CH1N	ADC_IN6 OPA2_VOUT

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
							UART2_RX EVENTOUT	
17	23	17	13	PA7	I/O	TT_a	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM1_CH1N COMP2_OUT TIM17_CH1 I2C2_SCL PWM1_CH1 UART2_TX EVENTOUT	ADC_IN7 OPA2_VINP
-	24	18	-	PC4	I/O	TT_a	TIM4_CH1 I2S1_MCK PWM1_BKIN UART2_TX EVENTOUT	ADC_IN14
-	25	19	-	PC5	I/O	TT_a	PWM1_CH2 UART2_RX EVENTOUT	ADC_IN15 OPA2_VINM WKUP5
18	26	20	14	PB0	I/O	TT_a	TIM3_CH3 TIM1_CH2N I2S1_MCK SPI1_MISO PWM3_ETR_LS UART1_RX EVENTOUT	ADC_IN8
19	27	21	15	PB1	I/O	TT_a	TIM3_CH4 TIM1_CH3N SPI2_SCK/I2S2_CK SPI1_MOSI/I2S1_SD PWM1_CH1 PWM3_ETR_HS EVENTOUT	ADC_IN9 COMP1_INP
20	28	22	16	PB2	I/O	FT	TIM3_ETR I2C1_SMBA	-

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
							PWM1_CH1N PWM3_CH2 EVENTOUT	
21	29	23	-	PB10	I/O	FT	I2C2_SCL TIM2_CH3 OPA2_COMP_OUT SPI2_SCK/I2S2_CK LPTIM1_IN1 PWM3_ETR_HS UART2_TX EVENTOUT	-
22	30	24	-	PB11	I/O	FT	I2C2_SDA TIM2_CH4 TIM15_ETR LPTIM1_IN2 UART2_RX EVENTOUT	-
23	31	-	-	V_{SS}	G	-	-	-
24	32	25	5	V_{CC}	S	-	-	-
25	33	-	-	PB12	I/O	FT	SPI2_NSS/I2S2_WS TIM1_BKIN TIM15_BKIN I2C2_SMBA SPI1_NSS/I2S1_WS PWM4_CH1 EVENTOUT	-
26	34	26	-	PB13	I/O	FT	SPI2_SCK/I2S2_CK TIM15_CH1N TIM1_CH1N I2C2_SCL SPI1_SCK/I2S1_CK LPTIM1_ETR PWM4_CH2 USART1_RX EVENTOUT	-

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
27	35	27	17	PB14	I/O	FT	SPI2_MISO TIM15_CH1 TIM1_CH2N I2C2_SDA SPI1_MISO LPTIM1_OUT PWM2_CH1N PWM4_CH3 USART1_TX EVENTOUT	-
28	36	28	-	PB15	I/O	FT	SPI2_MOSI/I2S2_SD TIM15_CH2 TIM1_CH3N TIM15_CH1N SPI1_MOSI/I2S1_SD PWM2_CH1 PWM4_CH4 EVENTOUT	-
-	37	-	-	PC6	I/O	TT	TIM3_CH1 I2C1_SCL TIM1_CH1 I2S2_MCK PWM1_CH2N EVENTOUT	-
-	38	-	-	PC7	I/O	TT	TIM3_CH2 I2C1_SDA TIM1_CH2 I2S2_MCK SPI2_SCK/I2S2_CK PWM3_CH2N LPUART1_RX EVENTOUT	-
-	39	-	-	PC8	I/O	TT	TIM3_CH3 TIM1_CH3 PWM3_CH1N	-

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
							LPUART1_TX EVENTOUT	
-	40	-	-	PC9	I/O	TT	TIM3_CH4 I2C2_SDA TIM1_CH4 I2C1_SDA PWM2_ETR_LS EVENTOUT	-
29	41	29	18	PA8	I/O	FT	MCO TIM15_ETR TIM1_CH1 I2C2_SCL PWM1_CH1N UART1_TX USART1_CK EVENTOUT	-
30	42	30	19	PA9	I/O	TT	TIM15_BKIN TIM1_CH2 I2C1_SCL I2C2_SMBA PWM2_CH1N PWM3_CH1 USART1_TX EVENTOUT	COMP2_INP
31	43	31	20	PA10	I/O	TT_a	TIM17_BKIN TIM1_CH3 I2C1_SDA SPI2_SCK/I2S2_CK SPI1_SCK/I2S1_CK LPTIM1_IN1 PWM2_ETR_LS USART1_RX EVENTOUT	-
32	44	32	21	PA11	I/O	FT	TIM1_CH4 COMP1_OUT	-

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
							I2C2_SCL I2C1_SMBA LPTIM1_IN2 PWM4_CH1 USART1_CTS EVENTOUT	
33	45	33	22	PA12	I/O	FT	TIM1_ETR COMP2_OUT I2C2_SDA TIM4_ETR PWM2_CH3 USART1_RTS_DE EVENTOUT	-
34	46	34	23	PA13	I/O	FT	SWDIO_JTMS IR_OUT OPA2_COMP_OUT I2C1_SDA SPI2_MISO SPI1_MISO PWM2_CH4 EVENTOUT	-
35	47	35	-	PD6	I/O	TT	I2C2_SCL PWM2_BKIN PWM3_CH4 LPUART1_RX EVENTOUT	-
36	48	36	25	PD7[3][4]	I/O	TT_a	I2C2_SDA SPI1_MISO TIM1_CH2 PWM1_ETR_LS PWM2_CH2N LPUART1_TX EVENTOUT	VREFBUF_OUT
37	49	37	24	PA14	I/O	FT	SWCLK_JTCK I2C1_SMBA SPI2_MOSI/I2S2_SD	-

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
							SPI1_MOSI/I2S1_SD LPTIM1_ETR PWM4_CH2 UART1_TX EVENTOUT	
38	50	38	25	PA15(4)	I/O	FT	JTDI TIM2_ETR TIM2_CH1 SPI2_NSS/I2S2_WS SPI1_NSS/I2S1_WS LPTIM1_OUT PWM3_BKIN UART1_RX LPUART1_RTS_DE EVENTOUT	-
-	51	-	-	PC10	I/O	TT	TIM15_ETR PWM1_CH4 PWM2_CH2N UART2_TX LPUART1_TX EVENTOUT	-
-	52	-	-	PC11	I/O	TT	PWM1_CH4 PWM3_CH2 UART2_RX LPUART1_RX EVENTOUT	-
-	53	-	-	PC12	I/O	TT	TIM4_CH2 PWM3_CH3 EVENTOUT	-
-	54	-	-	PD2	I/O	FT	TIM3_ETR PWM2_CH1 EVENTOUT	-
39	55	39	26	PB3	I/O	FT	JTDO SPI1_SCK/I2S1_CK TIM2_CH2	-

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
							SPI2_SCK/I2S2_CK PWM3_CH2N USART1_RTS_DE EVENTOUT	
40	56	40	27	PB4	I/O	FT	JTRST SPI1_MISO TIM3_CH1 TIM17_BKIN SPI2_MISO I2C1_SDA PWM4_CH4 USART1_CTS EVENTOUT	-
41	57	41	28	PB5	I/O	FT	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM16_BKIN I2C1_SMBA SPI2_MOSI/I2S2_SD PWM2_ETR_HS USART1_CK EVENTOUT	WKUP3
42	58	42	29	PB6	I/O	FT	I2C1_SCL TIM16_CH1N I2S1_MCK PWM3_CH3 USART1_TX EVENTOUT	-
43	59	43	30	PB7	I/O	FT	I2C1_SDA TIM17_CH1N PWM4_CH3 USART1_RX LPUART1_CTS EVENTOUT	-

Packages				Pin name	Pin type	I/O structure	Pin functions	
LQFP48 C1	LQFP64 R1	QFN48 C2	QFN32 K1				Alternate functions	Alternate functions
44	60	44	31	PD3-BOOT0	I/O	FT	TIM4_CH2 PWM2_CH2 EVENTOUT	-
45	61	45	-	PB8	I/O	FT	I2C1_SCL TIM16_CH1 COMP1_OUT PWM3_CH4 USART1_TX EVENTOUT	-
46	62	46	-	PB9	I/O	FT	IR_OUT I2C1_SDA TIM17_CH1 COMP2_OUT SPI2_NSS/I2S2_WS I2S1_MCK UART1_TX EVENTOUT	-
47	63	47	32	PD8	I/O	FT	TIM4_CH3 PWM2_CH2 EVENTOUT	-
48	64	48	-	PD9	I/O	FT	SPI1_NSS/I2S1_WS TIM4_CH3 PWM3_BKIN USART1_RX EVENTOUT	-

1. Available functions depend on the specified device. If multiple peripherals share the same I/O pin, to avoid conflicts between these functions, only one peripheral can be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
2. The main functions after the first backup domain is powered on. After this it depends on the contents of the backup registers, even after a reset (as these registers are not controlled by the main area reset).
3. When using the V_{REFBUF} function, a 1 µF external capacitor must be connected to PD7, and this pin cannot be simultaneously used as a general-purpose I/O.

4. Two IO ports are lead out on the same pin, only one of the IO ports can be used at the same time, and the other IO must be configured in analog mode (MODEy [1: 0] is 0B11).

3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	-	TIM2_ETR	TIM2_CH1	-	COMP1_OUT	TIM1_ETR	-	TIM4_CH4	-	PWM1_ETR_LS	-	-	UART1_RX	LPUART1_TX	EVEN-TOUT
PA1	-	-	-	TIM2_CH2	I2C2_SDA	OPA2_COMP_OUT	TIM15_CH1N	I2C1_SMBA	TIM4_ETR	-	PWM1_BKIN	PWM2_CH1	-	-	LPUART1_RX	EVEN-TOUT
PA2	-	TIM15_CH1	-	TIM2_CH3	-	COMP2_OUT	-	-	-	-	PWM1_CH2	-	-	UART1_TX	-	EVEN-TOUT
PA3	-	TIM15_CH2	-	TIM2_CH4	I2C2_SCL	-	I2S2_MCK	-	-	-	PWM1_CH2N	PWM2_BKIN	-	UART1_RX	-	EVEN-TOUT
PA4	-	SPI1_NSS/ I2S1_WS	-	-	-	-	I2C1_SCL	SPI2_NSS/ I2S2_WS	-	-	PWM1_CH1	-	-	-	-	EVEN-TOUT
PA5	-	SPI1_SCK /I2S1_CK	TIM2_ETR	TIM2_CH1	-	OPA2_COMP_OUT	-	-	-	LPTIM1_IN1	PWM1_CH1N	-	-	UART2_RX	USART1_CK	EVEN-TOUT
PA6	-	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	COMP1_OUT	TIM16_CH1	I2S2_MCK	TIM4_CH1	-	PWM1_ETR_HS	-	PWM3_CH1N	UART2_RX	-	EVEN-TOUT
PA7	-	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	-	COMP2_OUT	TIM17_CH1	-	I2C2_SCL	-	PWM1_CH1	-	-	UART2_TX	-	EVEN-TOUT
PA8	MCO	TIM15_ETR	-	TIM1_CH1	-	-	-	-	I2C2_SCL	-	PWM1_CH1N	-	-	UART1_TX	USART1_CK	EVEN-TOUT
PA9	-	TIM15_BKIN	-	TIM1_CH2	-	I2C1_SCL	-	-	I2C2_SMBA	-	-	PWM2_CH1N	PWM3_CH1	USART1_TX	-	EVEN-TOUT
PA10	-	TIM17_BKIN	-	TIM1_CH3	-	I2C1_SDA	-	SPI2_SCK/ I2S2_CK	SPI1_SCK/ I2S1_CK	LPTIM1_IN1	-	PWM2_ETR_LS	-	USART1_RX	-	EVEN-TOUT
PA11	-	-	-	TIM1_CH4	-	COMP1_OUT	I2C2_SCL	I2C1_SMBA	-	LPTIM1_IN2	-	-	PWM4_CH1	USART1_CTS	-	EVEN-TOUT
PA12	-	-	-	TIM1_ETR	-	COMP2_OUT	I2C2_SDA	-	TIM4_ETR	-	-	PWM2_CH3	-	USART1_RTS_DE	-	EVEN-TOUT
PA13	SWDIO_JTMS	-	IR_OUT	-	-	OPA2_COMP_OUT	I2C1_SDA	SPI2_MISO	SPI1_MISO	-	-	PWM2_CH4	-	-	-	EVEN-TOUT
PA14	SWCLK_JTCK	-	-	-	-	-	I2C1_SMBA	SPI2_MOSI/ I2S2_SD	SPI1_MOSI/ I2S1_SD	LPTIM1_ETR	-	-	PWM4_CH2	UART1_TX	-	EVEN-TOUT
PA15	JTDI	-	TIM2_ETR	TIM2_CH1	-	-	-	SPI2_NSS/ I2S2_WS	SPI1_NSS/ I2S1_WS	LPTIM1_OUT	-	-	PWM3_BKIN	UART1_RX	LPUART1_RTS_DE	EVEN-TOUT

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	-	TIM3_CH3	TIM1_CH2N	-	-	-	I2S1_MCK	SPI1_MISO	-	-	-	PWM3_ETR_LS	UART1_RX	-	EVEN-TOUT
PB1	-	-	TIM3_CH4	TIM1_CH3N	-	-	-	SPI2_SCK/ I2S2_CK	SPI1_MOSI/ I2S1_SD	-	PWM1_CH1	-	PWM3_ETR_HS	-	-	EVEN-TOUT
PB2	-	-	TIM3_ETR	-	-	-	-	-	I2C1_SMBA	-	PWM1_CH1N	-	PWM3_CH2	-	-	EVEN-TOUT
PB3	JTDO	SPI1_SCK/ I2S1_CK	-	TIM2_CH2	-	-	-	SPI2_SCK/ I2S2_CK	-	-	-	-	PWM3_CH2N	USART1_RTS_DE	-	EVEN-TOUT
PB4	JTRST	SPI1_MISO	TIM3_CH1	-	-	-	TIM17_BKIN	SPI2_MISO	I2C1_SDA	-	-	-	PWM4_CH4	USART1_CTS	-	EVEN-TOUT
PB5	-	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-	SPI2_MOSI/ I2S2_SD	-	-	-	PWM2_ETR_HS	-	USART1_CK	-	EVEN-TOUT
PB6	-	-	I2C1_SCL	TIM16_CH1N	-	-	-	I2S1_MCK	-	-	-	-	PWM3_CH3	USART1_TX	-	EVEN-TOUT
PB7	-	-	I2C1_SDA	TIM17_CH1N	-	-	-	-	-	-	-	-	PWM4_CH3	USART1_RX	LPUART1_CTS	EVEN-TOUT
PB8	-	-	I2C1_SCL	TIM16_CH1	-	COMP1_OUT	-	-	-	-	-	-	PWM3_CH4	USART1_TX	-	EVEN-TOUT
PB9	-	IR_OUT	I2C1_SDA	TIM17_CH1	-	COMP2_OUT	SPI2_NSS/ I2S2_WS	I2S1_MCK	-	-	-	-	-	UART1_TX	-	EVEN-TOUT
PB10	-	-	I2C2_SCL	TIM2_CH3	-	OPA2_COMP_OUT	SPI2_SCK/ I2S2_CK	-	-	LPTIM1_IN1	-	-	PWM3_ETR_HS	UART2_TX	-	EVEN-TOUT
PB11	-	-	I2C2_SDA	TIM2_CH4	-	-	TIM15_ETR	-	-	LPTIM1_IN2	-	-	-	UART2_RX	-	EVEN-TOUT
PB12	-	SPI2_NSS/ I2S2_WS	-	TIM1_BKIN	-	-	TIM15_BKIN	I2C2_SMBA	SPI1_NSS/ I2S1_WS	-	-	-	PWM4_CH1	-	-	EVEN-TOUT
PB13	-	SPI2_SCK/ I2S2_CK	TIM15_CH1N	TIM1_CH1N	-	-	I2C2_SCL	-	SPI1_SCK/ I2S1_CK	LPTIM1_ETR	-	-	PWM4_CH2	USART1_RX	-	EVEN-TOUT
PB14	-	SPI2_MISO	TIM15_CH1	TIM1_CH2N	-	-	I2C2_SDA	-	SPI1_MISO	LPTIM1_OUT	-	PWM2_CH1N	PWM4_CH3	USART1_TX	-	EVEN-TOUT
PB15	-	SPI2_MOSI/ I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	SPI1_MOSI/ I2S1_SD	-	-	PWM2_CH1	PWM4_CH4	-	-	EVEN-TOUT

3.3. Alternate functions selected through GPIOC_AFR registers for port C

Table 3-5 Port C alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0		-	I2C2_SCL	-		-	-	-	I2C1_SCL	-	-	PWM2_ETR_HS	-	-	-	EVENTOUT
PC1		-	I2C2_SDA	-		-	SPI1_MOSI/I2S1_SD	SPI2_MOSI/I2S2_SD	I2C1_SDA	-	PWM1_ETR_HS	-	-	-	-	EVENTOUT
PC2		-	SPI2_MISO	-	I2S2_MCK	-	-	-	-	-	PWM1_CH3	-	-	-	-	EVENTOUT
PC3		-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	PWM1_CH3	-	-	-	-	EVENTOUT
PC4	-	-	-	-	-	TIM4_CH1	-	I2S1_MCK	-	-	PWM1_BKIN	-	-	UART2_TX	-	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	PWM1_CH2	-	-	UART2_RX	-	EVENTOUT
PC6	-	TIM3_CH1	I2C1_SCL	TIM1_CH1	-	-	I2S2_MCK	-	-	-	PWM1_CH2N	-	-	-	-	EVENTOUT
PC7	-	TIM3_CH2	I2C1_SDA	TIM1_CH2	-	-	I2S2_MCK	SPI2_SCK/I2S2_CK	-	-	-	-	PWM3_CH2N	-	LPUART1_RX	EVENTOUT
PC8	-	TIM3_CH3	-	TIM1_CH3	-	-	-	-	-	-	-	-	PWM3_CH1N	-	LPUART1_TX	EVENTOUT
PC9	-	TIM3_CH4	I2C2_SDA	TIM1_CH4	-	-	-	-	I2C1_SDA	-	-	PWM2_ETR_LS	-	-	-	EVENTOUT
PC10	-	-	-	-	-	-	TIM15_ETR	-	-	-	PWM1_CH4	PWM2_CH2N	-	UART2_TX	LPUART1_TX	EVENTOUT
PC11	-	-	-	-	-	-	-	-	-	-	PWM1_CH4	-	PWM3_CH2	UART2_RX	LPUART1_RX	EVENTOUT
PC12	-	-	-	-	-	TIM4_CH2	-	-	-	-	-	-	PWM3_CH3	-	-	EVENTOUT
PC13	-	-	-	-	-	-	-	-	-	-	PWM1_CH2	-	-	-	-	EVENTOUT
PC14	-	-	-	-	-	-	-	-	-	-	PWM1_CH3	-	-	-	-	EVENTOUT
PC15	-	-	-	-	-	-	-	-	-	-	PWM1_CH4	-	-	-	-	EVENTOUT

3.4. Alternate functions selected through GPIOD_AFR registers for port D

Table 3-6 Port D alternate function mapping

PortD	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	-	-	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PD1	-	-	-	TIM1_CH2N	-	-	-	SPI2_NSS/ I2S2_WS	-	-	-	-	-	-	-	EVENTOUT
PD2	-	TIM3_ETR	-	-	-		-	-	-	-	-	PWM2_CH1	-	-	-	EVENTOUT
PD3	-	-	-	-	-	TIM4_CH2	-	-	-	-	-	PWM2_CH2	-	-	-	EVENTOUT
PD4	-	-	I2C1_SDA	TIM2_CH1	-		-	-	-	-	-	PWM2_CH3	-	-	-	EVENTOUT
PD5	-	-	I2C1_SCL	TIM2_CH2	-		-	-	-	-	-	PWM2_CH4	PWM3_CH1	-	-	EVENTOUT
PD6	-	I2C2_SCL	-	-	-		-	-	-	-	-	PWM2_BKIN	PWM3_CH4	-	LPUART1_RX	EVENTOUT
PD7	-	I2C2_SDA	SPI1_MISO	TIM1_CH2	-		-	-	-	-	PWM1_ETR_LS	PWM2_CH2N	-	-	LPUART1_TX	EVENTOUT
PD8	-	-	-	-	-	TIM4_CH3	-	-	-	-	-	PWM2_CH2	-	-	-	EVENTOUT
PD9	-	SPI1_NSS/ I2S1_WS	-	-	-	TIM4_CH3	-	-	-	-	-	-	PWM3_BKIN	USART1_RX	-	EVENTOUT
PD10	-	-	-	-	-	TIM4_CH4	-	-	-	-	-	-	PWM3_ETR_LS	USART1_TX	-	EVENTOUT
PD11	MCO	-	-	-	-		-	-	-	-	-	-	-	-	-	EVENTOUT

4. Memory mapping

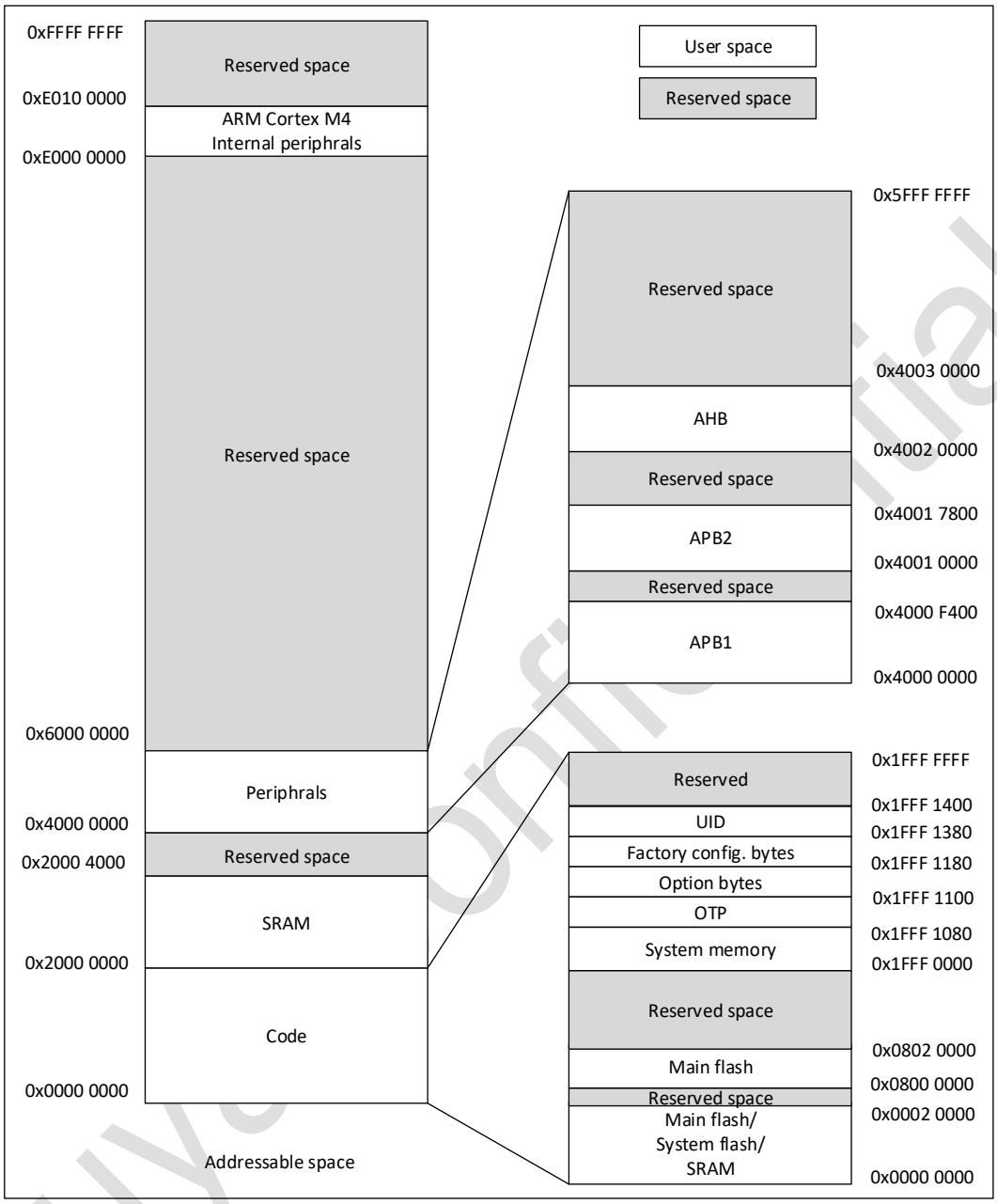


Figure 4-1 Memory mapping

Table 4-1 Memory boundary address

Type	Boundary address	Size	Storage area	Descriptions
SRAM	0x2002 4000-0x3FFF FFFF	511 MB	Reserved	1. When the CPU reads and writes this space, a Response error is generated, and then a HardFault exception is entered. 2. A TEIF status bit is generated when DMA accesses
	0x2000 0000-0x2000 3FFF	16 KB	SRAM	If the hardware power-on configuration SRAM is 128 KB, the SRAM address space is 0x2000 0000-0x2000 3FFF
Code	0x1FFF 1380 - 0x1FFF 13FF	128 Bytes	UID bytes	Unique ID
	0x1FFF 1180 - 0x1FFF 137F	512 Bytes	Factory config. bytes	-
	0x1FFF 1100 - 0x1FFF 117F	128 Bytes	Option bytes	Option bytes information
	0x1FFF 1080 - 0x1FFF 10FF	128 Bytes	OTP	-
	0x1FFF 0000 - 0x1FFF 107F	4.125 KB	System memory	Store Boot loader
	0x0802 0000-0x1FFE FFFF	127 MB	Reserved	-
	0x0800 0000-0x0801 FFFF	128 KB	Main flash memory	-
	0x0002 0000-0x07FF FFFF	127 MB	Reserved	1. When the CPU reads and writes this space, a Response error is generated, and then a HardFault exception is entered. 2. A TEIF status bit is generated when DMA accesses
	0x0000 0000-0x0001 FFFF	128 KB	Depending on the Boot configuration selection: 1）Main flash memory 2) System memory 3）SRAM	-

1. The address is marked as Reserved, which cannot be written, read as 0, and a response error is generated.

Table 4-2 Peripheral register address

Memory boundary address	Peripherals	Bus	Max. CPU frequency
0x4002 5000 - 0x4002 FFFF	Reserved	AHB	128 MHz
0x4002 4C00 - 0x4002 4FFF	GPIOD		
0x4002 4800 - 0x4002 4BFF	GPIOC		
0x4002 4400 - 0x4002 47FF	GPIOB		
0x4002 4000 - 0x4002 43FF	GPIOA		
0x4002 3400 - 0x4002 3FFF	Reserved		
0x4002 3000 - 0x4002 33FF	CRC		
0x4002 2400 - 0x4002 2FFF	Reserved		
0x4002 2000 - 0x4002 23FF	FMC		
0x4002 1400 - 0x4002 1FFF	Reserved		
0x4002 1000 - 0x4002 13FF	RCC		
0x4002 0400 - 0x4002 0FFF	Reserved		
0x4002 0000 - 0x4002 03FF	DMA1		
0x4001 7C00 - 0x4001 FFFF	Reserved	APB2	128 MHz
0x4001 7800 - 0x4001 7BFF	PWM4		
0x4001 7400 - 0x4001 77FF	Reserved		
0x4001 7000 - 0x4001 73FF	OPA		
0x4001 6C00 - 0x4001 6FFF	COMP		
0x4001 6400 - 0x4001 6BFF	Reserved		
0x4001 6000 - 0x4001 63FF	TIMER17		
0x4001 5C00 - 0x4001 5FFF	TIMER16		
0x4001 5800 - 0x4001 5BFF	TIMER15		
0x4001 4400 - 0x4001 57FF	Reserved		
0x4001 4000 - 0x4001 43FF	PWM3		
0x4001 3C00 - 0x4001 3FFF	Reserved		
0x4001 3800 - 0x4001 3BFF	USART1		
0x4001 3400 - 0x4001 37FF	Reserved		
0x4001 3000 - 0x4001 33FF	SPI1		
0x4001 2C00 - 0x4001 2FFF	TIMER1		
0x4001 2800 - 0x4001 2BFF	Reserved		
0x4001 2400 - 0x4001 27FF	ADC1		
0x4001 0800 - 0x4001 23FF	Reserved		
0x4001 0400 - 0x4001 07FF	EXTI		
0x4001 0000 - 0x4001 03FF	SYSCFG		
0x4000 8400 - 0x4000 FFFF	Reserved	APB1	128 MHz
0x4000 8000 - 0x4000 83FF	LPUART1		
0x4000 7C00 - 0x4000 7FFF	LPTIM1		
0x4000 7400 - 0x4000 7BFF	Reserved		
0x4000 7000 - 0x4000 73FF	PWR		
0x4000 6000 - 0x4000 6FFF	Reserved		
0x4000 5800 - 0x4000 5FFF	I2C2		
0x4000 5400 - 0x4000 57FF	I2C1		
0x4000 5000 - 0x4000 53FF	UART2		

Memory boundary address	Peripherals	Bus	Max. CPU frequency
0x4000 4C00 - 0x4000 4FFF	UART1		
0x4000 4400 - 0x4000 4BFF	Reserved		
0x4000 4000 - 0x4000 43FF	PWM2		
0x4000 3C00 - 0x4000 3FFF	Reserved		
0x4000 3800 - 0x4000 3BFF	SPI2/I2S2		
0x4000 3400 - 0x4000 37FF	PWM1		
0x4000 3000 - 0x4000 33FF	IWDG		
0x4000 2C00 - 0x4000 2FFF	WWDG		
0x4000 2800 - 0x4000 2BFF	RTC		
0x4000 1800 - 0x4000 27FF	Reserved		
0x4000 1400 - 0x4000 17FF	TIMER7		
0x4000 1000 - 0x4000 13FF	TIMER6		
0x4000 0C00 - 0x4000 0FFF	Reserved		
0x4000 0800 - 0x4000 0BFF	TIMER4		
0x4000 0400 - 0x4000 07FF	TIMER3		
0x4000 0000 - 0x4000 03FF	TIMER2		

1. In the above table , the reserved address cannot be written, read back is 0, and a hardfault is generated.
2. Support 32 bits word, half-word and byte access.
3. Support 32 bits word and half-word access.

5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A(max) (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization,the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 σ).

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C and V_{CC}= 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated (mean ±2 σ).

5.1.3. Power supply scheme

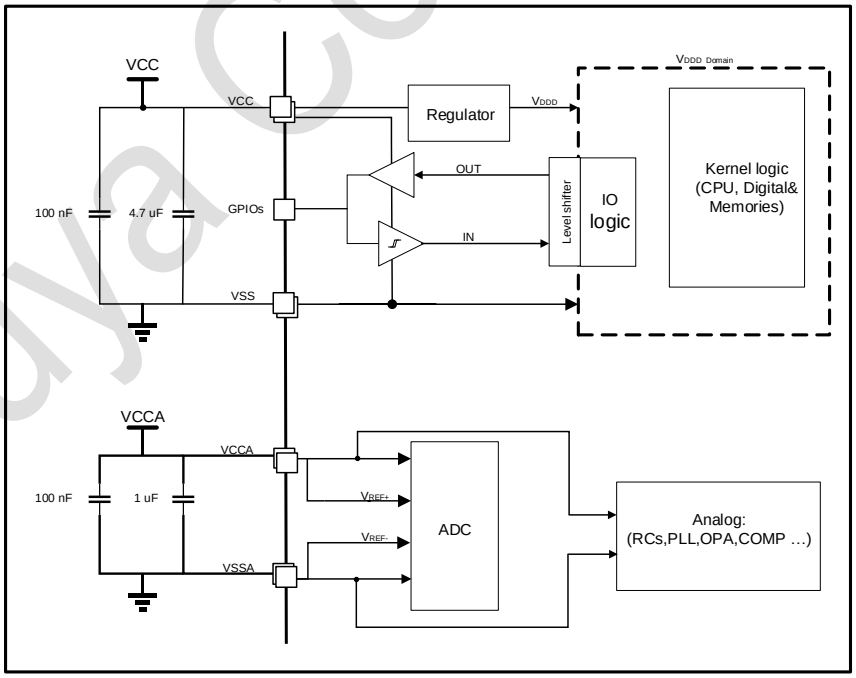


Figure 5-1 Power supply scheme

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}-V_{SS}	External supply voltage (including V_{CC}, V_{CCA})	-0.3	4.0	V
VIN(2)	FT, NRST I/O input voltage	V_{SS}-0.3	5.5	V
	TT, TT_a I/O input voltage	V_{SS}-0.3	4.0	
$\|DV_{CCx}\|$	Voltage variation between different V_{CC} pins	-	50	mV
$\|V_{SSX}$ -$V_{SS}\|$	Voltage variation between different pins	-	50	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. Maximum VIN must always follow allowable maximum injection current limits as per the table.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC}/V_{CCA} power lines (source)(1)	170	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	170	
$\Sigma I_{IO(PIN)}$(2)	Total output current sunk by sum of all I/Os and control pins	120	
	Total output current sourced by sum of all I/Os and control pins	120	
I_{IO}(2)	Output current sunk by any I/O and control pin	30	
	Output current sourced by any I/Os and control pin	30	
$I_{INJ(PIN)}$(3)	Injected current on 5 V-tolerant pins(4)	-5/+0	
	Injected current on any other pin(5)	±5	
$\Sigma I_{INJ(PIN)}$(6)	Total injected current (sum of all I/O and control pins)	±25	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.
3. Negative injection disturbs the analog performance of the device.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by V_{IN}>V_{CCA} while a negative injection is induced by V_{IN} < V_{SS}.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 5-3 Thermal characteristics

Symbol	Descriptions	Max	Unit
T_{STG}	Storage temperature range	-65 to 150	℃
T_J	Maximum junction temperature	150	℃

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	Range 1	0	128	MHz
		Range 2	0	96	
		Range 3	0	64	
f_{PCLK1}	APB1 clock frequency	Range 1	0	128	
		Range 2	0	96	
		Range 3	0	64	
f_{PCLK2}	APB2 clock frequency	Range 1	0	128	
		Range 2	0	96	
		Range 3	0	64	
V_{CC}	Operating voltage	-	2.0	3.6	V
V_{CCA}	Operating voltage of analog circuit	Must be the same potential as V_{CC}	2.0	3.6	V
V_{IN}	FT, NRST I/O input voltage	-	V_{SS}-0.3	5.5	V
	TT, TT_a I/O input voltage	-	V_{SS}-0.3	3.6	
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	110	℃

5.3.2. Operating conditions at power-on / power-down

Table 5-5 Operating conditions at power-on / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	10	∞	μs/V
	V_{CC} fall rate	-	20	∞	

5.3.3. Reset and power control block characteristics

Table 5-6 Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}(3)	PVD threshold	PLS[2: 0] = 000 (rising edge)	Reserved			V
		PLS[2: 0] = 000 (falling edge)				
		PLS[2: 0] = 001 (rising edge)	2.08(2)	2.18	2.28	
		PLS[2: 0] = 001 (falling edge)	2.0	2.08	2.18(2)	
		PLS[2:0]=010 (Rising edge)	2.27(2)	2.37	2.47	
		PLS[2:0]=010 (Falling edge)	2.17	2.27	2.37(2)	
		PLS[2:0]=011 (Rising edge)	2.46(2)	2.56	2.66	
		PLS[2:0]=011 (Falling edge)	2.36	2.46	2.56(2)	
		PLS[2:0]=100 (Rising edge)	2.64(2)	2.74	2.84	
		PLS[2:0]=100 (Falling edge)	2.54	2.64	2.74(2)	
		PLS[2:0]=101 (Rising edge)	2.73(2)	2.83	2.93	
		PLS[2:0]=101 (Falling edge)	2.63	2.73	2.83(2)	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PLS[2:0]=110 (Rising edge)	2.83(2)	2.93	3.03	
		PLS[2:0]=110 (Falling edge)	2.73	2.83	2.93(2)	
		PLS[2:0]=111 (Rising edge)	Reserved			
		PLS[2:0]=111 (Falling edge)				
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.86	1.92	1.98	V
		Falling edge	1.82	1.88	1.94	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(4)	POR reset temporization	-	1	2.5	4.5	ms

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. The LSI or LSE clock needs to be turned on for PVD to take effect.
4. The reset temporization is measured from the power-on (POR reset) to the instant when the first instruction is read by the user application code.

5.3.4. Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. All the run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{CC} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 28 MHz, 1 wait state from 28 to 60 MHz, 3 wait states from 60 to 90 MHz, 4 wait states from 90 to 120 MHz and 5 wait states from 120 to 128 MHz).
- Unless otherwise specified, typical data is based on T_A = 25 °C and V_{CC} = 3.3 V, The command prefetch function is turned on, When the peripheral is turned on: $f_{PCLK}1/2 = f_{HCLK}$.

Note: The command prefetch function must be set before setting the clock and bus frequency division.

Table 5-7 Current consumption in Run mode from Flash, ACC enabled

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	While(1)	Flash	All peripheral clocks enabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	16.4	21.4	21.7	mA
					PLL	96 MHz	12.5	16.4	16.6	
					PLL	64 MHz	8.5	11.2	11.4	
					HSI	48 MHz	6.5	8.6	8.8	
					HSI	24 MHz	3.3	4.5	4.7	
					HSI	16 MHz	2.4	3.4	3.6	
					HSI	8 MHz	1.5	2.1	2.4	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	12.0	15.8	15.9	
					PLL	64 MHz	8.2	10.8	10.9	
					HSI	48 MHz	6.2	8.3	8.4	
					HSI	24 MHz	3.2	4.3	4.5	
					HSI	16 MHz	2.3	3.2	3.4	
					HSI	8 MHz	1.4	2.1	2.3	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	7.8	10.3	10.6	
					HSI	48 MHz	6.0	7.9	8.2	
					HSI	24 MHz	3.1	4.1	4.3	
					HSI	16 MHz	2.2	3.1	3.3	
					HSI	8 MHz	1.4	2.0	2.2	
			All peripheral clock disabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	10.4	13.7	13.8	
					PLL	96 MHz	8.0	10.6	10.7	
					PLL	64 MHz	5.5	7.3	7.5	
					HSI	48 MHz	4.2	5.7	5.9	
					HSI	24 MHz	2.2	3.0	3.2	
					HSI	16 MHz	1.7	2.4	2.6	
					HSI	8 MHz	1.1	1.7	1.9	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	7.7	10.2	10.3	
					PLL	64 MHz	5.3	7.1	7.2	
					HSI	48 MHz	4.1	5.5	5.6	
					HSI	24 MHz	2.1	2.9	3.1	

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
					HSI	16 MHz	1.6	2.3	2.5	
					HSI	8 MHz	1.1	1.6	1.8	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	5.1	6.8	6.9	
					HSI	48 MHz	3.9	5.3	5.4	
					HSI	24 MHz	2.0	2.8	3.0	
					HSI	16 MHz	1.5	2.2	2.4	
					HSI	8 MHz	1.0	1.5	1.7	

1. Data based on characterization results, not tested in production.
2. PLL is enabled when f_{HCLK} > 48 MHz.

Table 5-8 Current consumptionin Run mode from Flash, ACC disabled

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	While(1)	Flash	All peripheral clocks enabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	14.9	19.5	19.7	mA
					PLL	96 MHz	11.3	14.9	15.1	
					PLL	64 MHz	7.7	10.2	10.4	
					HSI	48 MHz	5.9	7.9	8.1	
					HSI	24 MHz	3.3	4.5	4.6	
					HSI	16 MHz	2.4	3.3	3.5	
					HSI	8 MHz	1.5	1.8	2.3	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	10.9	14.3	14.5	
					PLL	64 MHz	7.4	9.8	10.0	
					HSI	48 MHz	5.7	7.6	7.7	
					HSI	24 MHz	3.1	4.3	4.5	
					HSI	16 MHz	2.3	3.2	3.4	
					HSI	8 MHz	1.4	1.7	2.2	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	7.1	9.4	9.6	
					HSI	48 MHz	5.4	7.3	7.4	
					HSI	24 MHz	3.0	4.1	4.3	
					HSI	16 MHz	2.2	3.1	3.2	
					HSI	8 MHz	1.4	1.6	2.2	
			All peripheral clock disabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	8.9	11.8	11.9	
					PLL	96 MHz	6.8	9.1	9.2	
					PLL	64 MHz	4.7	6.3	6.5	
					HSI	48 MHz	3.6	5.0	5.2	
					HSI	24 MHz	2.1	3.0	3.2	
					HSI	16 MHz	1.6	2.3	2.5	

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
					HSI	8 MHz	1.1	1.6	1.8	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	6.6	8.7	8.9	
					PLL	64 MHz	4.5	6.1	6.2	
					HSI	48 MHz	3.5	4.8	4.9	
					HSI	24 MHz	2.1	2.9	3.1	
					HSI	16 MHz	1.6	2.2	2.4	
					HSI	8 MHz	1.0	1.5	1.7	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	4.4	5.9	6.0	
					HSI	48 MHz	3.4	4.6	4.7	
					HSI	24 MHz	2.0	2.8	2.9	
					HSI	16 MHz	1.5	2.2	2.3	
					HSI	8 MHz	1.0	1.5	1.7	

1. Data based on characterization results, not tested in production.
2. PLL is enabled when f_{HCLK} > 48 MHz.

Table 5-9 Current consumption in Run mode (SRAM)

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	While(1)	SRAM	All peripheral clocks enabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	15.6	20.4	20.7	mA
					PLL	96 MHz	11.9	15.6	15.8	
					PLL	64 MHz	8.1	10.7	10.9	
					HSI	48 MHz	6.1	8.2	8.4	
					HSI	24 MHz	3.4	4.6	4.8	
					HSI	16 MHz	2.5	3.4	3.6	
					HSI	8 MHz	1.5	2.2	2.4	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	11.4	15.0	15.2	
					PLL	64 MHz	7.8	10.3	10.4	
					HSI	48 MHz	5.9	7.8	8.0	
					HSI	24 MHz	3.2	4.4	4.6	
					HSI	16 MHz	2.4	3.3	3.5	
					HSI	8 MHz	1.4	2.1	2.3	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	7.5	9.9	10.0	
					HSI	48 MHz	5.7	7.5	7.7	
					HSI	24 MHz	3.1	4.2	4.4	
					HSI	16 MHz	2.3	3.2	3.3	
					HSI	8 MHz	1.4	2.0	2.2	
			All peripheral clock disabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	9.1	12.0	12.2	
					PLL	96 MHz	7.0	9.3	9.5	
					PLL	64 MHz	4.8	6.5	6.6	
					HSI	48 MHz	3.7	5.0	5.2	
					HSI	24 MHz	2.2	3.0	3.2	
					HSI	16 MHz	1.6	2.4	2.6	

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
					HSI	8 MHz	1.1	1.6	1.9	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	6.8	9.0	9.1	
					PLL	64 MHz	4.7	6.2	6.4	
					HSI	48 MHz	3.5	4.8	5.0	
					HSI	24 MHz	2.1	2.9	3.1	
					HSI	16 MHz	1.6	2.3	2.5	
					HSI	8 MHz	1.1	1.6	1.8	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	4.5	6.0	6.1	
					HSI	48 MHz	3.4	4.6	4.8	
					HSI	24 MHz	2.0	2.8	3.0	
					HSI	16 MHz	1.5	2.2	2.4	
					HSI	8 MHz	1.0	1.5	1.7	

1. Data based on characterization results, not tested in production.
2. PLL is enabled when f_{HCLK} > 48 MHz.

Table 5-10 Current consumption in Sleep mode

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	While(1)	Flash	All peripheral clocks enabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	10.1	13.3	13.5	mA
					PLL	96 MHz	7.8	10.3	10.4	
					PLL	64 MHz	5.3	7.1	7.3	
					HSI	48 MHz	4.1	5.5	5.7	
					HSI	24 MHz	2.3	3.3	3.5	
					HSI	16 MHz	1.8	2.1	2.7	
					HSI	8 MHz	1.2	1.7	1.9	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	7.5	9.9	10.0	
					PLL	64 MHz	5.1	6.8	7.0	
					HSI	48 MHz	3.9	5.3	5.5	
					HSI	24 MHz	2.3	3.1	3.3	
					HSI	16 MHz	1.7	2.0	2.6	
					HSI	8 MHz	1.1	1.6	1.9	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	4.9	6.6	6.7	
					HSI	48 MHz	3.8	5.1	5.2	
					HSI	24 MHz	2.2	3.0	3.2	
					HSI	16 MHz	1.6	1.9	2.5	
					HSI	8 MHz	1.1	1.6	1.8	
			All peripheral clock disabled	Range 1 MR_VSEL = 2'b00	PLL	128 MHz	3.4	4.6	4.8	
					PLL	96 MHz	2.7	3.7	3.9	
					PLL	64 MHz	2.0	2.7	2.9	
					HSI	48 MHz	1.5	2.2	2.4	
					HSI	24 MHz	1.1	1.6	1.8	

Symbol	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
	Code	Run	Peripherals	Voltage mode			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
					HSI	16 MHz	0.92	1.4	1.6	
					HSI	8 MHz	0.72	1.2	1.3	
				Range 2 MR_VSEL = 2'b10	PLL	96 MHz	2.7	3.6	3.7	
					PLL	64 MHz	1.9	2.6	2.8	
					HSI	48 MHz	1.5	2.1	2.3	
					HSI	24 MHz	1.0	1.5	1.7	
					HSI	16 MHz	0.89	1.3	1.5	
					HSI	8 MHz	0.70	1.1	1.2	
				Range 3 MR_VSEL = 2'b01	PLL	64 MHz	1.9	2.5	2.7	
					HSI	48 MHz	1.4	2.0	2.2	
					HSI	24 MHz	1.0	1.5	1.6	
					HSI	16 MHz	0.87	1.3	1.5	
					HSI	8 MHz	0.68	1.1	1.2	

1. Data based on characterization results, not tested in production.
2. PLL is enabled when f_{HCLK} > 48 MHz.

Table 5-11 Current consumptionn in Low power run mode from Flash, ACC enabled

Symbol	Parameter	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
		Code	Run	MR/LPR/DLPR	Peripherals			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in LP_RUN mode	While(1)	Flash	LPR	All peripheral clocks enabled	HSI	2 MHz	0.60	0.94	1.09	mA
						HSI	1 MHz	0.52	0.83	0.99	
						HSI	62.5 kHz	0.44	0.73	0.89	
					All peripheral clock disabled	HSI	2 MHz	0.51	0.82	0.97	
						HSI	1 MHz	0.46	0.76	0.91	
						HSI	62.5 kHz	0.42	0.70	0.86	

1. Data based on characterization results, not tested in production.

Table 5-12 Current consumptionn in Low power run mode from Flash, ACC disabled

Symbol	Parameter	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
		Code	Run	MR/LPR/DLPR	Peripherals			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in LP_RUN mode	While(1)	Flash	LPR	All peripheral clocks enabled	HSI	2 MHz	0.59	0.93	1.09	mA
						HSI	1 MHz	0.51	0.83	0.98	
						HSI	62.5 kHz	0.44	0.73	0.89	
					All peripheral clock disabled	HSI	2 MHz	0.51	0.81	0.97	
						HSI	1 MHz	0.46	0.75	0.91	
						HSI	62.5 kHz	0.42	0.73	0.86	

1. Data based on characterization results, not tested in production.

Table 5-13 Current consumptionn in Low power run mode from SRAM

Symbol	Parameter	Conditions				System clock	f_{HCLK}(2)	Typ(1)			Unit
		Code	Run	MR/LPR/DLPR	Peripherals			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in LP_RUN mode	While(1)	SRAM	LPR	All peripheral clocks enabled	HSI	2 MHz	0.60	0.85	1.10	mA
						HSI	1 MHz	0.51	0.78	0.99	
						HSI	62.5 kHz	0.44	0.72	0.59	
					All peripheral clock disabled	HSI	2 MHz	0.51	0.69	0.97	
						HSI	1 MHz	0.46	0.68	0.91	
						HSI	62.5 kHz	0.42	0.67	0.86	

1. Data based on characterization results, not tested in production.

Table 5-14 Current consumption in Low-power Sleep mode

Symbol	Parameter	Conditions			System clock	f_{HCLK}(2)	Typ(1)			Unit
		Code	MR/LPR/DLPR	Peripherals			T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Current in LP_SLEEP mode	While(1)	LPR	All peripheral clocks enabled	HSI	2 MHz	0.53	0.85	1.00	mA
					HSI	1 MHz	0.48	0.78	0.94	
					HSI	62.5 kHz	0.43	0.72	0.88	
				All peripheral clock disabled	HSI	2 MHz	0.43	0.69	0.83	
					HSI	1 MHz	0.42	0.68	0.82	
					HSI	62.5 kHz	0.41	0.67	0.80	

1. Data based on characterization results, not tested in production.

Table 5-15 Current consumption in (Stop0/Stop1/Stop2) mode

Symbol	Parameter	MR/LPR/DLPR	Conditions	Typ(1)			Unit
				T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{VCC}	Supply current in Stop0 mode	MR	RTC + IWDG + LPTIM with LSI	345	575	705	μA
			IWDG with LSI	345	575	705	
			LPTIM with LSI	345	575	705	
			RTC with LSI	345	575	705	
			Peripheral shutdown	345	575	705	
	Supply current in Stop1 mode	LPR	RTC + IWDG + LPTIM with LSI	135	300	430	
			IWDG with LSI	135	300	430	
			LPTIM with LSI	135	300	430	
			RTC with LSI	135	300	430	
			Peripheral shutdown	135	300	430	
	Supply current in Stop2 mode	DLPR	RTC + IWDG with LSI	15	95	170	
			IWDG with LSI	15	95	170	
			RTC+LSI	15	95	170	
			Peripheral shutdown	15	95	170	

1. Data based on characterization results, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5-16 Wake-up time from low-power mode

Symbol	Parameter[1]	Power Supply [2]	Conditions	Typ[3]	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-	-	5	6	CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	-	-	17	18	
t_{WUSTOP}	Wake up time from Stop 0mode to Run mode	MR	Run program in Flash, HSI (8 MHz) as system clock	7.0	7.5	μs
			Run program in SRAM, HSI (8 MHz) as system clock	4.5	5.5	
	Wake up time from Stop 1 mode to Run mode	LPR	Run program in Flash, HSI (8 MHz) as system clock	11.5	12.5	
			Run program in SRAM, HSI (8 MHz) as system clock	8.5	9.5	
	Wake up time from Stop 2 mode to Run mode	DLPR	Run program in Flash, HSI (8 MHz) as system clock	21.5	22.5	
			Run program in SRAM, HSI (8 MHz) as system clock	19.0	24.0	
	Wake up time from Stop 1 mode to Low power run mode	LPR	Run program in Flash, HSI (8 MHz) as system clock and HCLK is 2 M	11.5	12.5	
			Run program in SRAM, HSI (8 MHz) as system clock and HCLK is 2 M	9.0	10.0	
	Wake up time from Stop 2 mode to Low power run mode	DLPR	Run program in Flash, HSI (8 MHz) as system clock and HCLK is 2 M	17.5	18.5	
			Run program in SRAM, HSI (8 MHz) as system clock and HCLK is 2 M	17.0	22.0	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.
3. Data are based on HSI 8 M conditions.

Table 5-17 Regulator mode transition time[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{VOST}	Regulator transition time for switching from Range 3 to Range 2	-	5	7	μs
	Regulator transition time for switching from Range 3 to Range 1	-	5	7	
	Regulator transition time for switching from Range 2 to Range 1	-	5	7	

1. Guaranteed by design, not tested in production.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the device stops working, the corresponding I/O is used as a standard GPIO.

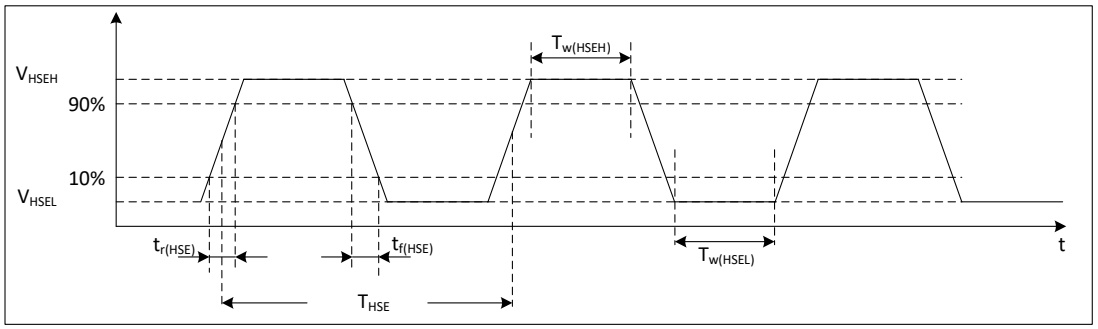


Figure 5-2 High-speed external clock timing diagram

Table 5-18 High-speed external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency(1)	-	1	-	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3*V_{CC}	
$t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ /$t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{CC}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

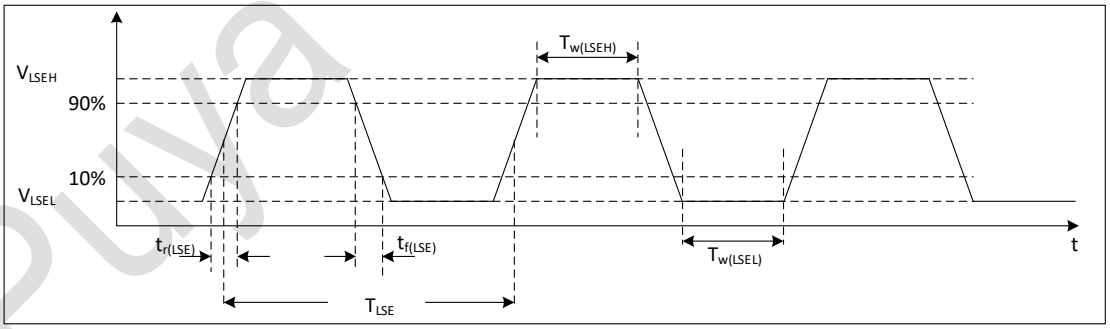


Figure 5-3 Low-speed external clock timing diagram

Table 5-19 Low-speed external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		0.7*V_{CC}	-	V_{CC}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	0.3*V_{CC}	
$t_{w(LSE)}$	OSC32_IN high or low time		450	-	-	ns
$t_{r(LSE)}$ /$t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	50	
$C_{in(LSE)}$	OSC32_IN input pin capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	40	-	60	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{CC}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-20 HSE oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-		4	-	32	MHz
R_F	Feedback resistor	-		-	385	-	kΩ
I_{CC}	HSE current consumption	CL = 12 pF @ 4 MHz, Rm = 100 Ω, HSE_DRV [1: 0] = 00		-	0.45	-	mA
		CL = 12 pF @ 8 MHz, Rm = 150 Ω, HSE_DRV [1: 0] = 00		-	0.47	-	
		CL = 12 pF @ 16 MHz, Rm = 70 Ω, HSE_DRV [1: 0] = 01			0.83		
		CL = 20 pF @ 24 MHz, Rm = 70 Ω, HSE_DRV [1: 0] = 10		-	1.56	-	
		CL = 10 pF @ 32 MHz, Rm = 40 Ω, HSE_DRV [1: 0] = 10		-	1.62	-	
g_m	Maximum critical crystal gm	Startup	HSE_DRV[1:0]=00	3.5	-	-	mA/V
			HSE_DRV[1:0]=01	5	-	-	
			HSE_DRV[1:0]=10	7.5	-	-	
			HSE_DRV[1:0]=11	10	-	-	
$t_{SU(HSE)}$(2)	Startup time	HSE_EN to rising edge of first duty cycle stable clock	C_L = 12 pF @ 4 MHz, Rm = 100 Ω, HSE_DRV [1: 0] = 00	-	1.4	-	ms
			C_L = 12 pF @ 8 MHz, Rm = 150 Ω, HSE_DRV [1: 0] = 00	-	2.27	-	
			C_L = 12 pF @ 16 MHz, Rm = 70 Ω, HSE_DRV [1: 0] = 01	-	0.28	-	
			C_L = 20 pF @ 24 MHz, Rm = 70 Ω, HSE_DRV [1: 0] = 10	-	0.68	-	
			C_L = 10 pF @ 32 MHz, Rm = 40 Ω, HSE_DRV [1: 0] = 10	-	0.24	-	

1. Evaluated by characterization, not tested in production.
2. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-21 LSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RF	Feedback resistor	-	-	5	-	MΩ
I_{CC}	LSE current consump-tion	C_L=6 pF，Rm=70 Ω，LSE_DRV[1:0]=00	-	600	-	nA
		C_L=6 pF，Rm=70 Ω，LSE_DRV[1:0]=01	-	700	-	
		C_L=12 pF，Rm=50 Ω，LSE_DRV[1:0]=10	-	1000	-	
		C_L=12 pF，Rm=50 Ω，LSE_DRV[1:0]=11	-	1500	-	
g_m	Maximum critical crys-tal gm	LSE_DRV[1:0]=00	2.5	-	-	μA/V
		LSE_DRV[1:0]=01	3.75	-	-	
		LSE_DRV[1:0]=10	8.5	-	-	
		LSE_DRV[1:0]=11	3.5	-	-	
$t_{SU(LSE)}$(2)	Startup time	C_L=6 pF，Rm=70 Ω，LSE_DRV[1:0]=00	-	1.10	-	s
		C_L=6 pF，Rm=70 Ω，LSE_DRV[1:0]=01	-	0.80	-	
		C_L=12 pF，Rm=50 Ω，LSE_DRV[1:0]=10	-	0.91	-	
		C_L=12 pF，Rm=50 Ω，LSE_DRV[1:0]=11	-	0.50	-	

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-22 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSI	HSI frequency	V_{CC} = 3.3 V，T_A = 25 °C	-	8.0	-	MHz
			-	16.0	-	
			-	24.0	-	
			-	48.0	-	
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
fTRIM(1)	HSI trimming accuracy	-	-	0.4	-	%
$\Delta_{Temp(HSI)}$	HSI frequency drift over temperature	V_{CC} = 2.0 to 3.6 V, T_A = 25 °C	-1	-	1	%
		V_{CC} = 2.0 to 3.6 V, T_A =-20 to 85 °C	-2	-	2	
		V_{CC} = 2.0 to 3.6 V, T_A =-40 to 105 °C	-4	-	4	
$t_{su(HSI)}$(2)	HSI oscillator startup time	8 MHz	-	1.5	-	μs
		16 MHz	-	0.7	-	
		24 MHz	-	0.7	-	
		48 MHz	-	0.7	-	
$I_{CC(HSI)}$(2)	HSI oscillator power consumption	8 MHz	-	130	-	μA
		16 MHz	-	180	-	
		24 MHz	-	230	-	
		48 MHz	-	280	-	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-23 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	40	-	kHz
$t_{su(LSI)}$(1)	LSI oscillator startup time	-	-	75	89.5	μs
DuCy(LSI)	Duty cycle	-	45	-	55	%
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	V_{CC} = 3.3 V，T_A = 25 °C	-4	-	4	%
		V_{CC} = 2.0 to 3.6 V, T_A = -20 to 85 °C	-12	-	12	
		V_{CC} = 2.0 to 3.6 V, T_A = -40 to 105 °C	-20	-	20	
$I_{CC(LSI)}$(1)	LSI oscillator power consumption	-	-	0.3	-	μA

1. Guaranteed by design, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-24 PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock	8	-	48	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}(2)	PLL multiplier output clock	48	128	144	MHz
t_{LOCK}	PLL lock time	-	25	50	μs
Jitter	Jitter	-	300	-	ps

1. Guaranteed by design, not tested in production.
2. The PLL output frequency (f_{PLL_OUT} < 96 MHz) must first be multiplied to exceed 96 MHz before being divided down to the target frequency.

5.3.10. Memory characteristics

Table 5-25 Memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
PE_{CYC}	Endurance	T_A = -40 - 85 °C	100	-	-	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 55 ℃	20	-	-	years
		1 kcycle at T_A = 85 ℃	15	-	-	
		1 kcycle at T_A = 105 ℃	10	-	-	
		10 kcycles at T_A = 55 ℃	10	-	-	
t_{PROG}	Page programming time	T_A = -40 to 105 °C	-	1.5	-	ms
t_{ERASE}	Page erase time	T_A = -40 to 105 °C	-	7	-	ms
t_{MERASE}	Mass erase time	T_A = -40 to 105 °C	-	7	-	ms

1. Guaranteed by design, not tested in production.

5.3.11. EFT characteristics

Table 5-26 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4A

5.3.12. ESD & LU characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Table 5-27 ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 ° C, JESD22-A114	-	-	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	T_A = 25 ° C, JESD22-C101	-	-	1000	V
LU	Overcurrent test	T_A = 25 ° C, JESD78A	-	-	±200	mA
	Overvoltage test		-	-	5.4	V

5.3.13. I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{CC} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

An out of range parameter indicates the failure: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of -5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Table 5-28 I/O current injection susceptibility

Symbol	Descriptions	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on 5V-tolerant pins	-5	0	mA
	Injected current on any other pin	-5	5	

5.3.14. I/O port characteristics

Table 5-29 IO port characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TT, TT_a	2.0 V≤V_{CC}≤ 3.6 V	-	-	0.39*V_{CC}-0.06	V
		FT	2.0 V≤V_{CC}≤ 3.6 V	-	-	0.35*V_{CC}-0.06	
V_{IH}	Input high level voltage	TT, TT_a	2.0 V≤V_{CC}≤ 3.6 V	0.49*V_{CC}+0.26	-	-	V
		FT	2.0 V≤V_{CC}≤ 3.6 V	0.53*V_{CC}+0.26	-	-	
V_{hys}(1)	Schmidt voltage hysteresis	TT, TT_a	-	-	200	-	mV
		FT		-	5% V_{CC}	-	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{Ikg}(2)	Input leakage current	TT, TT_a	$V_{SS}≤V_{IN}≤V_{CCD}$	-	-	±100	nA
		FT	$0<V_{IN}≤V_{CCD}$	-	-	±100	
			$V_{CCD}<V_{IN}≤V_{CCD}+1V$	-	-	2000	
			$V_{CCD}+1<V_{IN}≤5.5V$	-	-	±200	
R_{PU}(3)	Internal pull-up resistor	$V_{IN}=V_{SS}$		30	40	50	kΩ
R_{PD}(3)	Internal pull-down resistor	$V_{IN}=V_{CC}$		30	40	50	kΩ
C_{IO}	Pin capacitance	-		-	5	-	pF
$t_{ns(EXTI)}$(1)	Input filter width	ENI=1，ENS=1		3	5	10	ns
$t_{ns(I2C)}$(1)	I^2C Input filter width	ENI=1，EIIC=1		50	140	250	ns
$t_{ns(NRST)}$(1)	NRST input filter width	ENI=1，ENS=1		100	180	300	ns

1. Guaranteed by design, not tested in production.
2. If there is reverse current pouring in adjacent pins, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are designed to be a real resistor in series with a switchable PMOS/NMOS.

Output driving current

The GPIOs (general-purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH})

In the user application, the number of I/O pins, which can drive current must be limited to respect the absolute maximum rating.

- The sum of the currents sourced by all the I/Os on V_{CC}, plus the maximum Run consumption of the MCU sourced on V_{CC}, cannot exceed the absolute maximum rating ΣI_{VCC}.
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS}.

Output voltage

Unless otherwise specified, the parameters given in table below are derived from tests performed under ambient temperature and V_{CC} supply voltage conditions.

Table 5-30 Output voltage characteristics(3)

Symbol	Parameter	Conditions (2)	Min(1)	Typ	Max(1)	Unit
V_{OL}	Output low level voltage	2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +20 mA (Up to 6 pins are allowed to sink current simultaneously)	-	-	1.3	V
	Output low level voltage	2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +8 mA (Up to 8 pins are allowed to sink current simultaneously)	-	-	0.4	
		2.0 V ≤ V_{CC} ≤ 2.7 V, I_{IO} = +6 mA (Up to 8 pins are allowed to sink current simultaneously)	-	-	0.4	
V_{OH}	Output high level voltage	2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +20 mA (Up to 6 pins are allowed to output current simultaneously)	V_{CC}-1.3	-	-	V
	Output high level voltage	2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +8 mA (Up to 8 pins are allowed to output current simultaneously)	V_{CC}-0.4	-	-	
		2.0 V≤V_{CC}≤ 2.7 V，I_{IO} = +6 mA (Up to 8 pins are allowed to output current simultaneously)	V_{CC}-0.4	-	-	

1. Data based on characterization results, not tested in production.
2. The test conditions for driving all IOs is that GPIOx_OSPEEDR = 11.
3. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current Characteristics

5.3.15. ADC characteristics

Table 5-31 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog power supply	-	2.0	-	3.6	V
V_{REF+}	Positive reference voltage	V_{REF+} = V_{CCA}	V_{CCA}			V
		V_{REF}+ = V_{REFBUF}	-	1.024	-	V
			-	1.5	-	
			-	2.048	-	
			-	2.5	-	
			-	2.9	-	
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
I_{CCA}	V_{CCA} pin current	f_{ADC} = 16 MHz	-	1(1)	-	mA
		f_{ADC} = 32 MHz	-	1(1)	-	
		f_{ADC} = 48 MHz	-	1(1)	-	
f_{ADC}	ADC clock frequency	2.0 V≤V_{CCA}≤3.6 V	8	-	16	MHz
		2.4 V≤V_{CCA}≤3.6 V	8	-	32	
		3.0 V≤V_{CCA}≤3.6 V	8	-	48	
f_S(2)	Sampling rate	V_{CCA}≥2.0 V	0.5	-	1	Msps
		V_{CCA}≥2.4 V	0.5		2	
		V_{CCA}≥3.0 V	0.5	-	3	
V_{AIN}	Conversion voltage range	Single-ended mode	0	-	V_{REF+}	V
		Differential mode	-V_{REF+}	-	V_{REF+}	
R_{AIN}(2)	External Input Impedance(3)	-	-	-	100	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1.2	kΩ
C_{ADC}(2)	Internal sampling and holding capacitor	-	-	2.5	3	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 16 MHz	12			μs
		-	192			1/f_{ADC}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S(2)	Sampling time	f_{ADC} = 16 MHz	0.156	-	40.03	μs
		-	2.5	-	640.5	1/f_{ADC}
t_{samp_setup}	Sampling time for internal channels	-	20	-	-	μs
t_{STAB}(2)	Power-on Stabilization time	-	0	0	3	μs
t_{CONV}(2)	Total conversion time	f_{ADC} = 16 MHz	1	-	40.875	μs
		-	16 to 654			1/f_{ADC}

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. When using external triggering, an additional delay of 1/f_{PCLK2} is required.
   a) $R_{AIN} < - R_{ADC}\frac{T_S}{f_{ADC}\times C_{ADC}\times \ln(2^{N+2})}$
   b) The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution).

Table 5-32 R_{AIN} Max for f_{ADC} = 48 MHz(1)

Sampling period (T_S)	Sampling time (ts)	Maximum value of R_{AIN} (Ω)	
		Fast channel	Slow channel
2.5	39.06	100	N/A
6.5	101.56	330	100
12.5	195.31	680	470
24.5	382.81	1500	1200
47.5	742.19	2200	1800
92.5	1445.31	4700	3900
247.5	3867.19	12000	10000
640.5	10007.81	39000	33000

1. Guaranteed by design, not tested in production.

Table 5-33 ADC static characteristics (1)(2)(3)

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	2.0 V ≤ V_{REF+} = V_{CCA} ≤ 3.6 V 12-bit resolution f_{ADC} ≤ 48 MHz	Single-ended mode	-	±3.0	±5.0	LSB
			Differential mode	-	±4.0	±5.5	
EO	Offset error		Single-ended mode	-	±2.0	±3.0	
			Differential mode	-	±1.5	±2.0	
EG	Gain error		Single-ended mode	-	±1.5	±3.5	
			Differential mode	-	±2.5	±3.0	
ED	Differential linearity error		Single-ended mode	-	±0.8	±1.2	
			Differential mode	-	±0.9	±1.2	
EL	Integral linearity		Single-ended mode	-	±2.0	±3.5	
			Differential mode	-	±2.0	±3.5	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin.

It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-34 ADC static characteristics (1)(2)(3)

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	V_{CCA} = 2.0 to 3.6 V V_{REF+}= V_{REFBUF} 12-bit resolution f_{ADC} ≤ 32 MHz	Single-ended mode	-	±4.0	±7.5	LSB
			Differential mode	-	±3.0	±3.5	
EO	Offset error		Single-ended mode	-	±1.5	±2.5	
			Differential mode	-	±1.5	±3.0	
EG	Gain error		Single-ended mode	-	±1.5	±7.0	
			Differential mode	-	±2.0	±3.5	
ED	Differential linearity error		Single-ended mode	-	±1.0	±1.3	
			Differential mode	-	-0.8 to 1.1	±1.2	
EL	Integral linearity		Single-ended mode	-	±2.5	±4.0	
			Differential mode	-	±2.0	±3.0	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-35 ADC dynamic characteristics(1)(2)(3)

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	V_{REF+} = V_{CCA} =3.3 V f_{ADC} ≤ 48 MHz 12-bit resolution	Single-ended mode	10.1	11.2	-	bit
			Differential mode	10.6	11.5	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	62.4	69.1	-	dB
			Differential mode	65.7	71.1	-	
SNR	Signal to noise ratio		Single-ended mode	65.5	70.1	-	
			Differential mode	68.2	71.2	-	
SFDR	Spurious free dynamic range		Single-ended mode	66.6	76.3	-	
			Differential mode	70.7	81.8	-	
THD	Total harmonic distortion		Single-ended mode	-65.3	-75.7	-	
			Differential mode	-69.2	-79.2	-	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-36 ADC dynamic characteristics(1)(2)(3)

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	V_{CCA} = 2.0 to 3.6 V V_{REF+} = V_{REFBUF} = 1.024 V	Single-ended mode	9.3	9.8	-	bit
			Differential mode	10.1	10.7	-	

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
SINAD	Signal to noise and distortion ratio	f_{ADC} ≤ 32 MHz 12-bit resolution	Single-ended mode	58.2	60.7	-	dB
			Differential mode	62.7	66.4	-	
SNR	Signal to noise ratio		Single-ended mode	59.5	61.6	-	
			Differential mode	63.6	66.5	-	
SFDR	Spurious free dynamic range		Single-ended mode	65.9	70.5	-	
			Differential mode	71.7	83.4	-	
THD	Total harmonic distortion		Single-ended mode	-64.2	-77.9	-	
			Differential mode	-69.8	-82.7	-	
ENOB	Effective number of bits	V_{CCA} = 2.0 to 3.6 V V_{REF+} = V_{REFBUF} = 1.5 V f_{ADC} ≤ 32 MHz 12-bit resolution	Single-ended mode	9.7	10.3		bit
			Differential mode	10.5	10.9	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	60.6	63.7	-	dB
			Differential mode	65.0	67.6	-	
SNR	Signal to noise ratio		Single-ended mode	61.8	63.7	-	
			Differential mode	65.6	67.9	-	
SFDR	Spurious free dynamic range		Single-ended mode	69.2	87.6	-	
			Differential mode	74.4	84.2	-	
THD	Total harmonic distortion		Single-ended mode	-66.8	-83.5	-	
			Differential mode	-73.2	-82.0	-	
ENOB	Effective number of bits	V_{CCA} = 2.4 to 3.6 V V_{REF+} = V_{REFBUF} = 2.048 V f_{ADC} ≤ 32 MHz 12-bit resolution	Single-ended mode	10.0	10.5	-	bit
			Differential mode	10.8	11.2	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	62.4	65.0	-	dB
			Differential mode	66.7	69.3	-	
SNR	Signal to noise ratio		Single-ended mode	63.3	65.1	-	
			Differential mode	67.5	69.6	-	
SFDR	Spurious free dynamic range		Single-ended mode	71.3	84.7	-	
			Differential mode	79.5	84.6	-	
THD	Total harmonic distortion		Single-ended mode	-69.5	-81.9	-	
			Differential mode	-74.8	-80.8	-	
ENOB	Effective number of bits	V_{CCA}=2.8 to 3.6 V V_{REF+} = V_{REFBUF} = 2.5 V f_{ADC} ≤ 32 MHz 12-bit resolution	Single-ended mode	10.2	10.7	-	bit
			Differential mode	10.9	11.3	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	63.5	66.1	-	dB
			Differential mode	67.8	70.0	-	
SNR	Signal to noise ratio		Single-ended mode	64.3	66.4	-	
			Differential mode	68.7	70.2	-	
SFDR	Spurious free dynamic range		Single-ended mode	74.2	78.5	-	
			Differential mode	80.6	86.6	-	
THD	Total harmonic distortion		Single-ended mode	-71.6	-77.4	-	
			Differential mode	-75.3	-83.3	-	
ENOB	Effective number of bits	V_{CCA} = 3.2 to 3.6 V V_{REF+} = V_{REFBUF} = 2.9 V f_{ADC} ≤ 32 MHz 12-bit resolution	Single-ended mode	10.3	10.7	-	bit
			Differential mode	11.1	11.3	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	64.2	66.3	-	dB
			Differential mode	68.7	69.7	-	
SNR	Signal to noise ratio		Single-ended mode	65.3	67.0	-	
			Differential mode	69.2	70.2	-	

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
SFDR	Spurious free dynamic range		Single-ended mode	74.6	76.7	-	
			Differential mode	82.1	79.7	-	
THD	Total harmonic distortion		Single-ended mode	-70.7	-74.1	-	
			Differential mode	-78.5	-78.6	-	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

5.3.16. Comparator characteristics

Table 5-37 Comparator characteris (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CCA}	Comparator supply voltage	-		2.0	-	3.6	V
V_{IN}	Input voltage range	-		0	-	V_{CC}	V
t_{START}	Startup time	High-speed mode		-	-	5	µs
		Medium-speed mode		-	-	15	
t_D	Propagation delay	High-speed mode	200 mV step 100 mV over-drive	-	40	70	ns
			>200 mV step 100 mV over-drive	-	-	85	
		Medium-speed mode	200 mV step 100 mV over-drive	-	1	2.5	µs
			>200 mV step 100 mV over-drive	-	-	3.4	
	Propagation delay (OPA2 as comparator)	200 mV step 100 mV over-drive		-	1	3	
Voffset	Offset voltage	-		-	±10	-	mV
V_{hys}	Hysteresis voltage	No hysteresis		-	0	-	mV
		With hysteresis		-	20	-	
I_{CCA}	V_{CCA} supply current	High-speed mode	Static	-	450	720	µA
			With 50 kHz and ±100 mv overdrive square signal	-	450	-	
		Medium-speed mode	Static	-	10	20	
			With 50 kHz and ±100 mv overdrive square signal	-	12	-	
I_{sleep}	Sleep power consumption	-	-	-	10	-	nA

1. Guaranteed by design, not tested in production.

5.3.17. Operational amplifier characteristics

Table 5-38 Operational amplifier characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Supply voltage	-	2.2	3.3	3.6	V
VIN	Input voltage range	-	0	-	V_{CCA}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{os}	Offset voltage	25 °C, Output no load	-	-	±3	mV
		Full voltage, full temperature	-	-	±5	
I_{LOAD}	Driving current	-	-	-	2.5	mA
C_{LOAD}	Load capacitance	-	-	-	50	pF
R_{LOAD}	Load resistor	-	4	-	-	kΩ
CMRR	Common mode rejection ratio	Frequency: 1 kHz	-	60	-	dB
PSRR	Power supply rejection ratio (to V_{CCA}) (static DC measurement)	Frequency 1 kHz, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 kΩ, Vcom = V_{CCA}/2	-	80	-	dB
		Frequency 1 MHz, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 kΩ, Vcom = V_{CCA}/2	40	-	-	
		Frequency 10 MHz, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 kΩ, Vcom = V_{CCA}/2	20	-	-	
GBW	Bandwidth	200 mV ≤ Vout ≤ V_{CCA}-200 mV	5	10	-	MHz
SR	Slew rate (from 10% * V_{CCA} to 90% * V_{CCA})	CL = 50 pF	2.5	6.5	-	V/μ s
V_{OHSAT}	Maximum output saturation voltage	I_{LOAD} = max or R_{LOAD} = min, Input at V_{CCA}. Follow mode	V_{CCA}-100	-	-	mV
V_{OLSAT}	Minimum output saturation voltage	I_{LOAD} = max or R_{LOAD} = min, Input at 0. follow mode	-	-	100	mV
Φm	Phase margin	Follow mode, Vcom = V_{CCA}/2	55	65	-	°
GM	Gain margin	Follow mode, Vcom = V_{CCA}/2	8	-	-	dB
t_{SU}	Start up time (off to output 98% * V_{CCA})	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 k Ω, Follow mode	-	3	6	μs
eN	Voltage noise density	1 kHz, output resistive load 4 kΩ	-	250	-	uV/√Hz
		10 kHz, output resistive load 4 kΩ	-	90	-	
I_{CCA}	OPA supply current	No load, follow mode	-	1.8	2.5	mA

1. Guaranteed by design, not tested in production.

5.3.18. Temperature sensor characteristics

Table 5-39 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
TL[1]	V_{SENSE} linearity with temperature	-	±1	-	°C
Avg_Slope[1]	Average slope	2.4	2.6	2.8	mV/°C
V_{30}[1]	Voltage at 30 ℃	0.66	0.68	0.70	V
t_{START}[2]	Start up time	-	70	150	μs
t_{S_temp}[2][3]	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. The shortest sampling time can be determined in the application by multiple iterations.

5.3.19. Embedded internal voltage reference (V_{REFINT}) characteristics

Table 5-40 Embedded internal voltage reference (V_{REFINT}) characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{S\_vrefint}$[1]	ADC sampling time when reading the internal reference voltage	10	-	-	μs

Symbol	Parameter	Min	Typ	Max	Unit
t_{START}	Startup time	-	10	15	μs
T_{Coeff}(1)	Temperature coefficient of V_{REFINT}	-	100	-	ppm/℃

1. Guaranteed by design, not tested in production.

5.3.20. Embedded internal voltage reference (V_{REFBUF}) characteristics

Table 5-41 Embedded internal voltage reference (V_{REFBUF}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog power supply	1.024 V internal reference buffer	2.0	-	3.6	V
		1.5 V internal reference buffer	2.0	-	3.6	
		2.048 V internal reference buffer	2.4	-	3.6	
		2.5 V internal reference buffer	2.8	-	3.6	
		2.9 V internal reference buffer	3.2	-	3.6	
$V_{REF1024}$	1.024 V internal reference buffer	T_A = 25 °C，V_{CC} = 3.3 V	1.014	1.024	1.034	V
V_{REF15}	1.5 V internal reference buffer	T_A = 25 °C，V_{CC} = 3.3 V	1.485	1.5	1.515	V
$V_{REF2048}$	2.048 V internal reference buffer	T_A = 25 °C，V_{CC} = 3.3 V	2.028	2.048	2.068	V
V_{REF25}	2.5 V internal reference buffer	T_A = 25 °C，V_{CC} = 3.3 V	2.475	2.5	2.525	V
V_{REF29}	2.9 V internal reference buffer	T_A = 25 °C，V_{CC} = 3.3 V	2.871	2.900	2.929	V
$T_{coeff\_VREF-BUF}$(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 to 105 °C	-	100	-	ppm/°C
$I_{CCA(VREFBUF)}$	V_{CCA} consumption	-	-	350	450	μA

1. Guaranteed by design, not tested in production.

5.3.21. Timer characteristics

Table 5-42 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 128 MHz	-	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 128 MHz	-	-	MHz
Res_{TIM}	Timer resolution time	-	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 128 MHz	-	-	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 128 MHz	-	-	s

Table 5-43 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	

Prescaler	PR[2:0]	Min	Max	Unit
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-44 WWDG characteristics (timeout period at 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.22. Communication interfaces

5.3.22.1. I²C interface characteristics

I²C interface meets the requirements of the I²C bus specification and user manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz
- Fast-mode plus (Fm+): 1 MHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-45 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

The I²C timings requirements are specified by design when the I²C peripheral is properly configured. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not true open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{CC} is disabled, but is still present.

Table 5-46 I²C filter characteristics

Symbol	Parameter	Standard I²C(1)		Fast I²C(1)(2)		Fast plus I²C(1)(2)		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	µs
$t_{w(SCLH)}$	SCL clock high time	4	-	0.6	-	0.2	-	µs
$t_{su(SDA)}$	SDA setup time	2000	-	800	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	250	-	250	-	130	-	
$t_{r(SDA)}$ /$t_{r(SDL)}$	SDA and SCL rise time	-	1000	-	300	-	120	
$t_{f(SDA)}$ /$t_{f(SDL)}$	SDA and SCL fall time	-	300	-	300	-	120	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.2	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.2	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.2	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
C_b	Capacitive load for each bus line	-	400	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK} must be at least 4 MHz to achieve standard mode I²C frequencies. f_{PCLK} must be at least 8 MHz to achieve fast mode I²C frequencies. f_{PCLK} must be at least 4 MHz to achieve fast mode plus I²C frequencies.

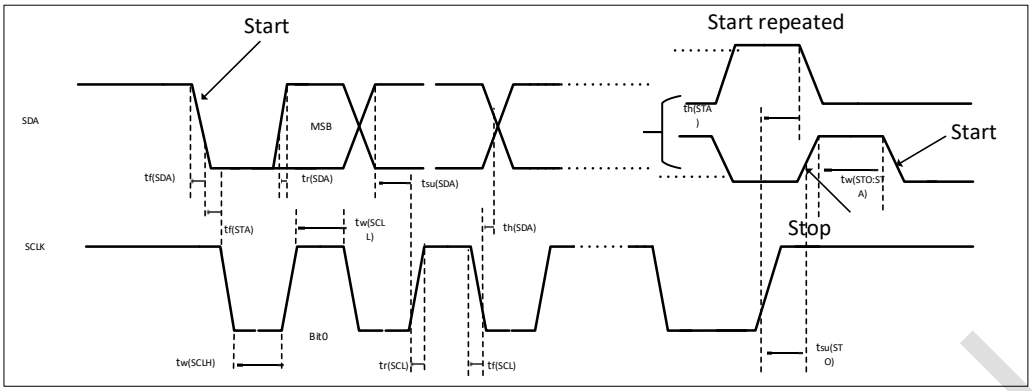


Figure 5-4 I²C bus timing diagram

5.3.22.2. SPI interface characteristics

Table 5-47 SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{SCK}/t_{c(SCK)}$	SPI clock frequency	Master mode Range 1	-	-	64	MHz
		Master mode Range 2	-	-	48	
		Master mode Range 3	-	-	32	
		slave mode Range 1	-	-	36	
		Slave mode Range 2	-	-	28	
		Slave mode Range 3	-	-	22	
$t_{su(NSS)}$	NSS setup time	Slave mode	$4*t_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2*t_{PCLK}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high level/low level time	Master mode, presc = 2	t_{pclk}-1	t_{pclk}	t_{pclk}+1	
$t_{su(MI)}$	Data input setup time	Master mode	6	-	-	
$t_{su(SI)}$		Slave mode	5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5.5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	
$t_{v(SO)}$	Data output valid time	Slave mode, presc = 2	-	9	12	
$t_{v(MO)}$		Master mode (after enable edge)	-	3.5	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	6(1)	-	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	-	

1. The Slave updates the data before the transmit edge if the SCK duty cycle sent by the Master is wide between the receive edge and the transmit edge.

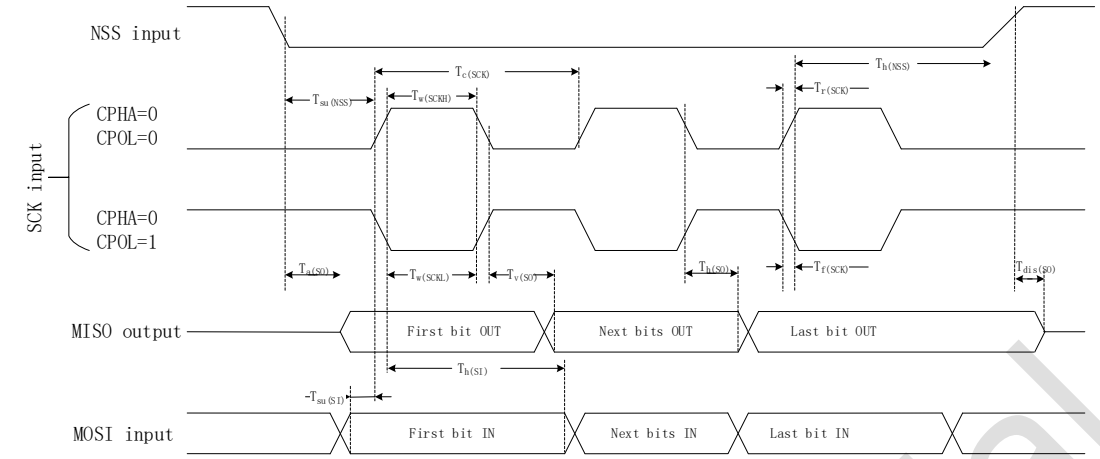


Figure 5-5 SPI timing diagram – slave mode and CPHA=0

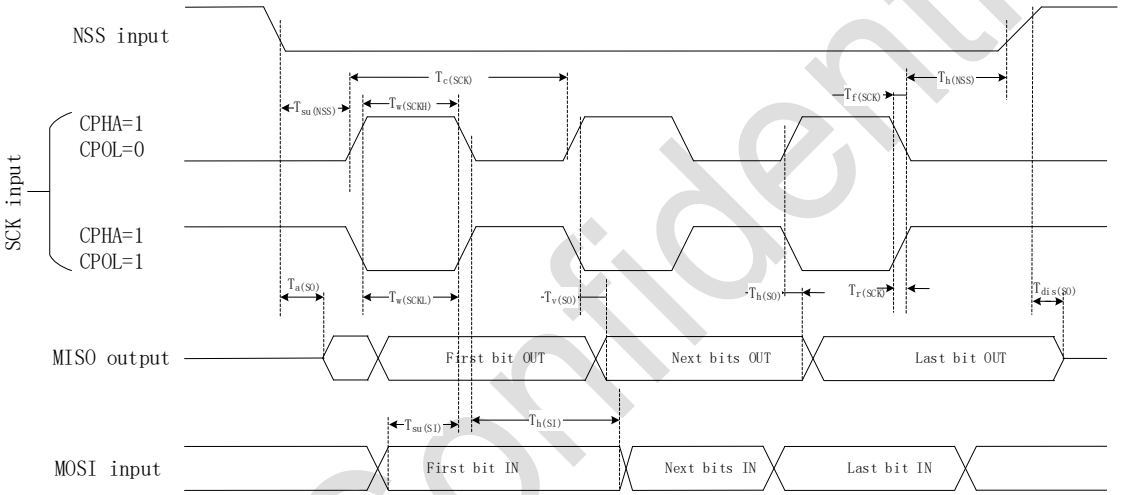


Figure 5-6 SPI timing diagram – slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS level: 0.3 V_{CC} and 0.7 V_{CC}

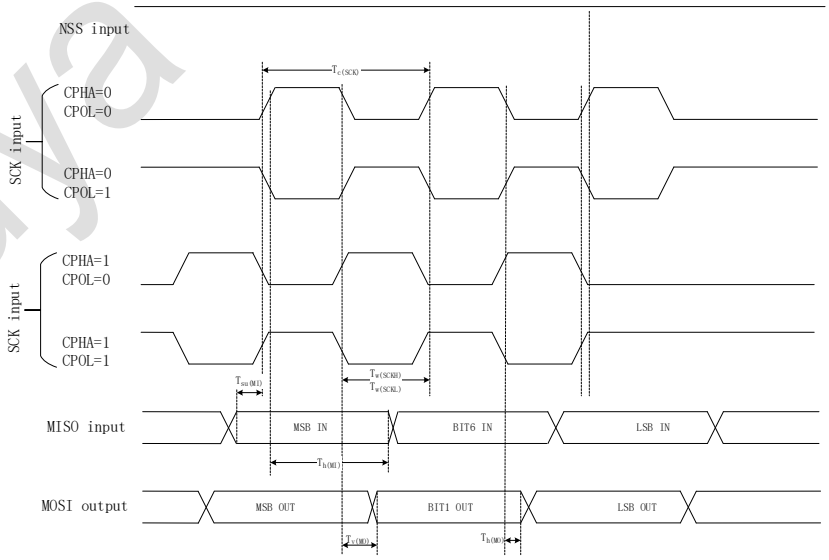


Figure 5-7 SPI timing diagram - slave mode(1)

1. Measurement points are done at CMOS level: 0.3 V_{CC} and 0.7 V_{CC}

5.3.22.3. I²S characteristics

Table 5-48 I²S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_S	I²S sampling frequency	-		8	192	kHz
f_{MCLK}	I²S main clock output	-		0.256 x f_S	0.256 x f_S	MHz
$f_{CK}1/t_{c(CK)}$	I²S clock frequency	Master data		-	64 x f_S	MHz
		Slave master		-	64 x f_S	
D_{CK}	I²S clock frequency duty cycle	Slave receiver		30	70	%
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load C_L = 50 pF		-	8	ns
$t_{v(WS)}$	WS valid time	Master mode		-	2	
$t_{h(WS)}$	WS hold time	Master mode		3	-	
		Slave mode		2	-	
$t_{su(WS)}$	WS setup time	Slave mode		4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver		3	-	
$t_{su(SD\_SR)}$		Slave receiver		4	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver		5	-	
$t_{h(SD\_SR)}$		Slave receiver		2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave receiver (after enable edge)	V_{CC} = 2.7 to 3.6 V	-	15	
			V_{CC} = 2.0 to 3.6 V	-	22	
$t_{v(SD\_MT)}$		Master receiver (after enable edge)		-	2	
$t_{h(SD\_ST)}$	Data output hold time	Slave receiver (after enable edge)		7	-	
$t_{h(SD\_MT)}$		Master receiver (after enable edge)		1	-	

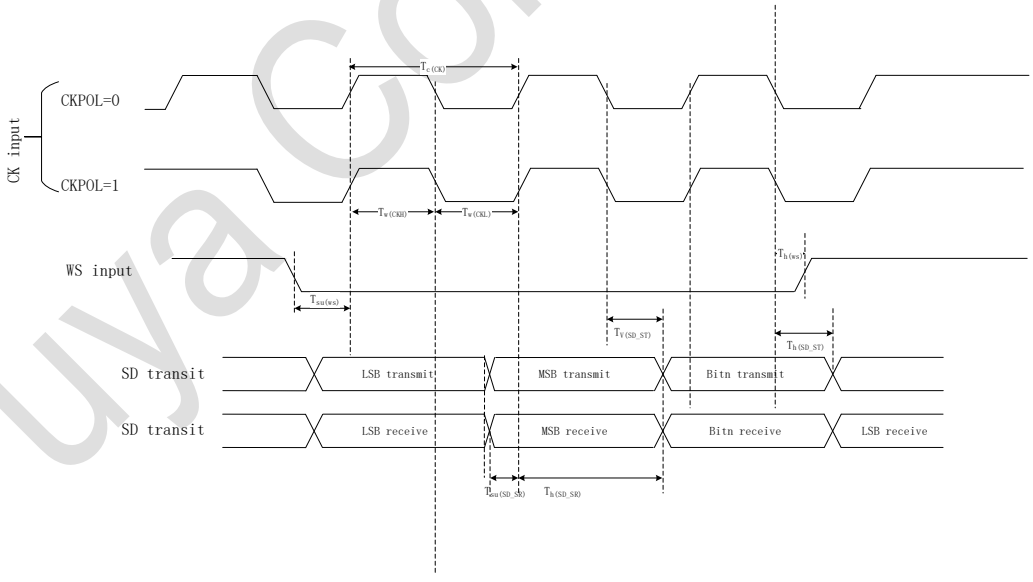


Figure 5-8 I²S slave timing diagram (Philips protocol)

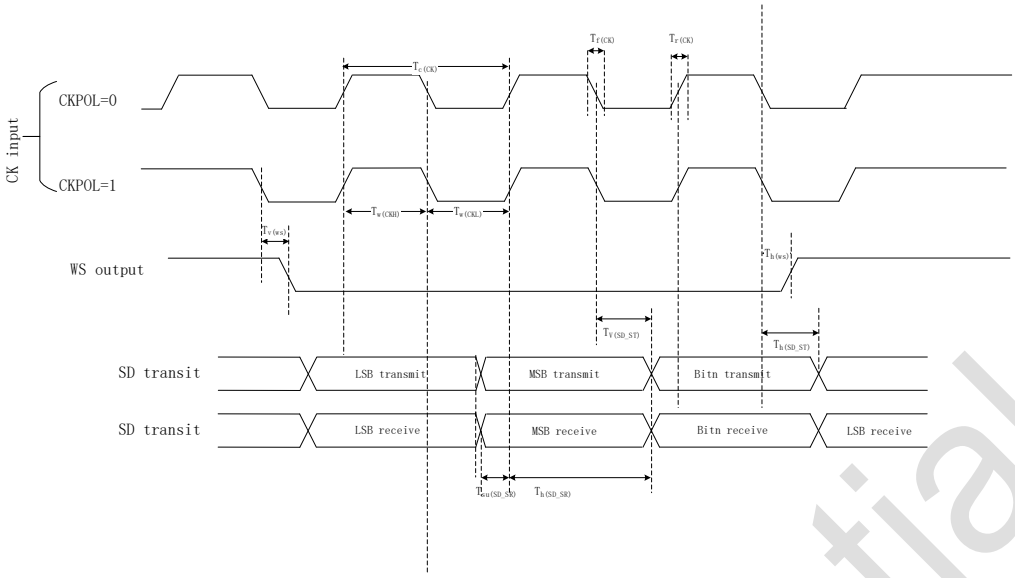
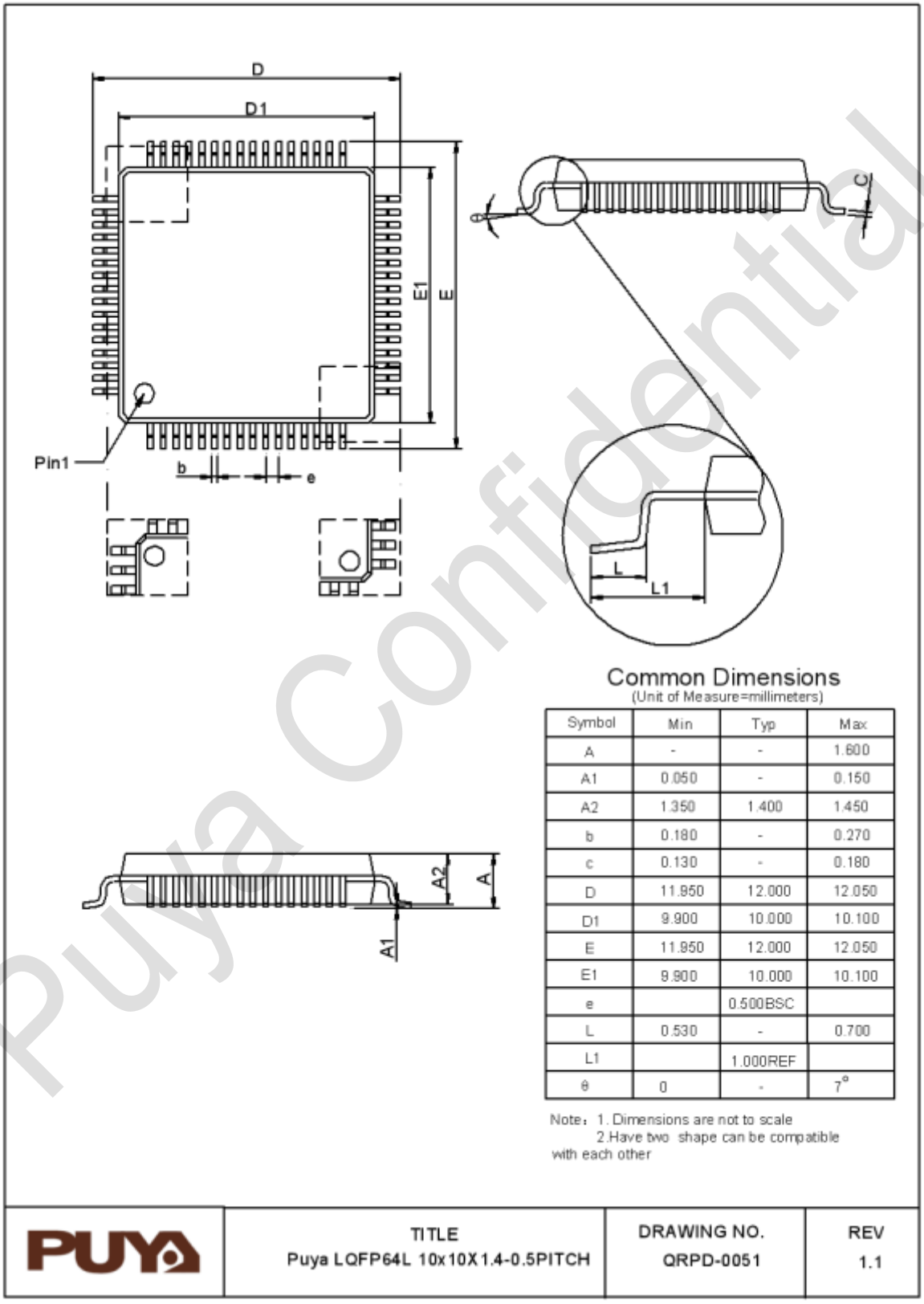


Figure 5-9 I²S master timing diagram (Philips protocol)

6. Package information

6.1. LQFP64 package size



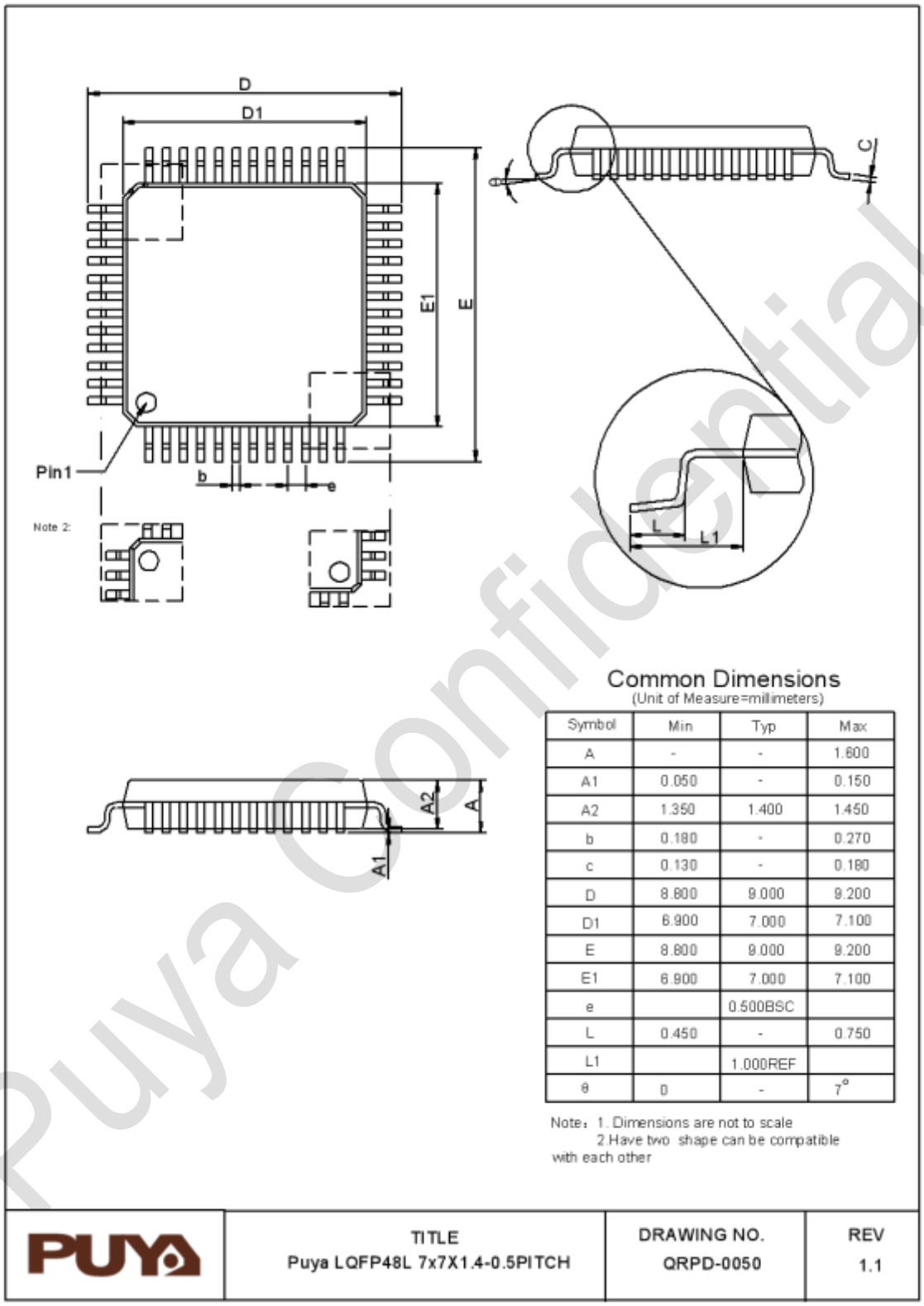
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	11.950	12.000	12.050
D1	9.900	10.000	10.100
E	11.950	12.000	12.050
E1	9.900	10.000	10.100
e		0.500BSC	
L	0.530	-	0.700
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP64L 10x10X1.4-0.5PITCH	QRPD-0051	1.1

6.2. LQFP48 package size



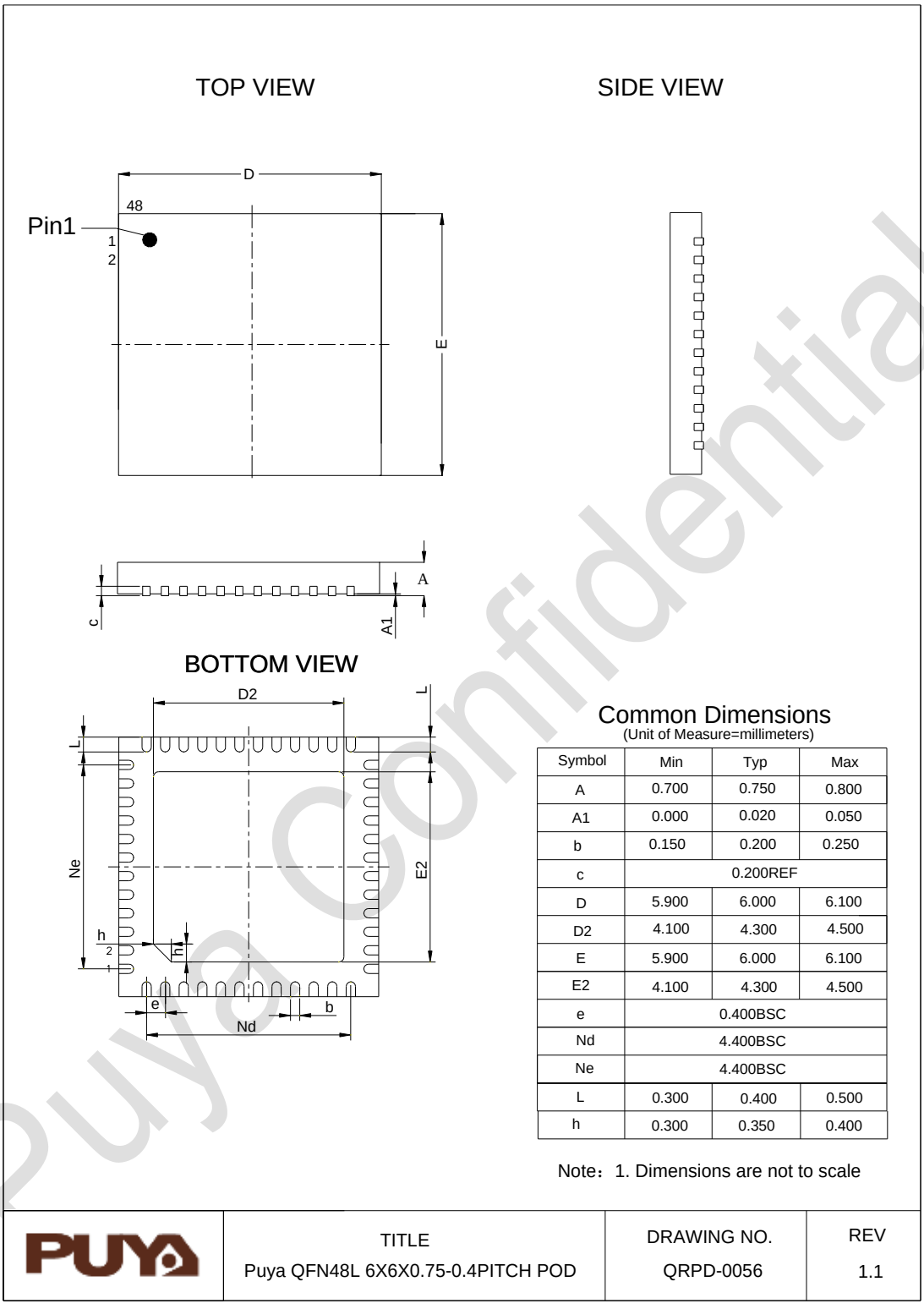
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP48L 7x7X1.4-0.5PITCH	QRPD-0050	1.1

6.3. QFN48 package size



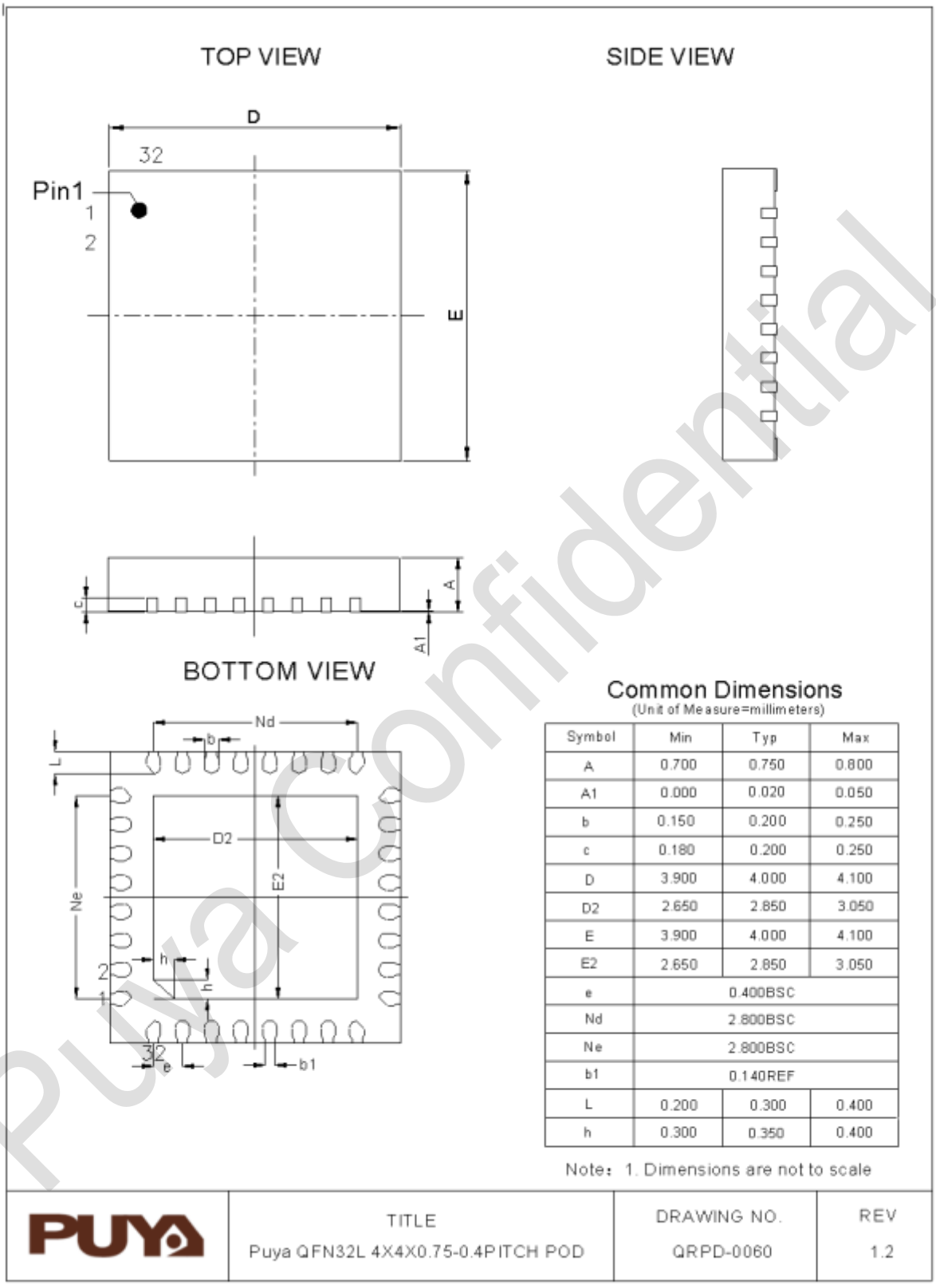
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.200REF	
D	5.900	6.000	6.100
D2	4.100	4.300	4.500
E	5.900	6.000	6.100
E2	4.100	4.300	4.500
e		0.400BSC	
Nd		4.400BSC	
Ne		4.400BSC	
L	0.300	0.400	0.500
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN48L 6X6X0.75-0.4PITCH POD	QRPD-0056	1.1

6.4. QFN32 (4*4) Package



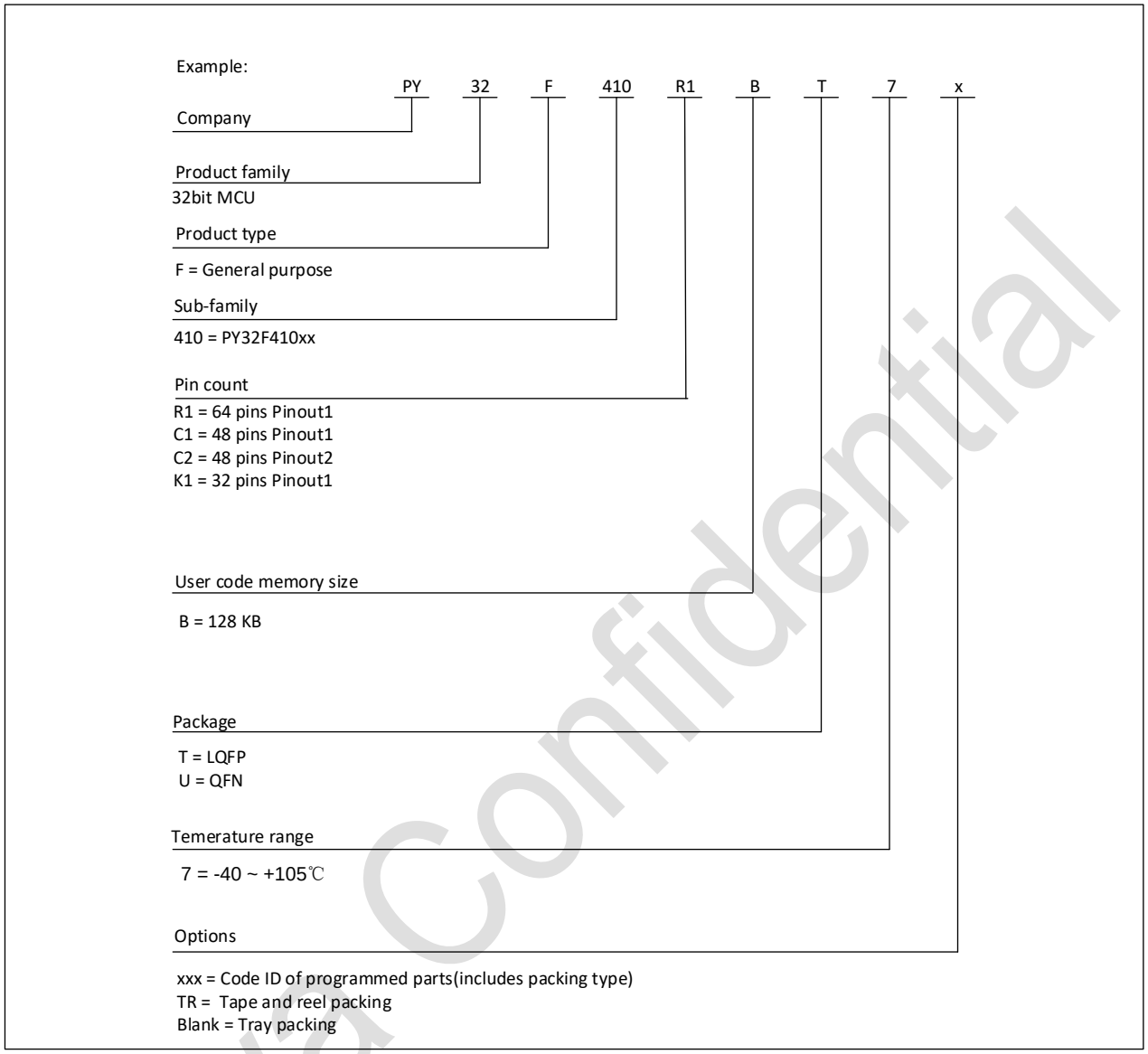
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.650	2.850	3.050
E	3.900	4.000	4.100
E2	2.650	2.850	3.050
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

Note: 1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.2

7. Ordering information



8. Version history

Version	Date	Descriptions
V0.1	2024.04.02	Beta version
V0.2	2024.04.20	Update Table 1-1, Table 3-1 and Table 3-2
V0.3	2024.05.10	Update product features and functionality descriptions
V0.4	2024.10.24	1. Update Introduction 2. Update partial format
V0.5	2025.02.24	Initial version
V0.6	2025.03.05	1. Added QFN48 and QFN32 packages 2. Update Table -522 internal high frequency clock source characteristics
V0.7	2025.03.31	Update Table 3-2 Pin Definitions
V0.8	2025.04.29	1. Added QFN48 pinput2 2. Updated Table 5-16 Low power mode wake-up time, Table 5-25 memory characteristics, Table 5-39 temperature sensor characteristics 3. Updated QFN32 (4 * 4) Package Dimension Drawing
V0.9	2025.07.30	Delete PY32F410C1BU7TR
V1.0	2025.08.15	1. Add voltage regulation function 2. Add ADC internal channel 3. Add data in section 5.3.4 and 5.3.5

Puya Semiconductor Co., Ltd.